

# 915GV-M5 1.0

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B	B	36		09/01/' 04
1.0	1.0	36		10/04/' 04

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DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	17	C/D/E/F	PREQ-0	PGNT-0
PCI2	18	D/E/F/G	PREQ-1	PGNT-1
PCI3	19	F/E/H/G	PREQ-2	PGNT-2
1394	20	D	PREQ-3	PGNT-3
LAN	21	E	PREQ-4	PGNT-4

PCB : 244 x 244 mm ; 4 layers

INTEL  
P4 Processor  
PSC, Tejas -  
LGA 775 pin

BW : 4.1GB/s @ FSB : 533MHz & Freq : 133MHz  
BW : 6.4GB/s @ FSB : 800MHz & Freq : 200MHz

SIZE : Min 128MB (ONE 256Mb X 16 Single-Sided DEVICES)  
SIZE : Max 4GB (Four 512Mb X 8 Double-Sided DEVICES)  
BW : 8.5GB/s @ DDR2 :400/533MHz  
BW : 6.4GB/s @ DDR : 333/400MHz

INTEL  
i910GL  
1210pin FC-BGA

DDIMM1: DDR Socket 184P  
DDIMM2 : DDR Socket 184P  
DDIMM3: DDR Socket 184P  
DDIMM4 : DDR Socket 184P

VGA (G only)

Analong Display  
RAMDAC: 400MHz  
Resolutions Up To 2048x1536@75Hz

USB1 2 ports  
USB2 2 ports  
USB3 2 ports  
USB4 2 ports  
USBLAN 8 ports

USB V2.0

INTEL  
ICH6  
609pin EPGA

BW : 133MB/s @Freq : 33MHz

PCI1 Slot 120pin @ AD17  
PCI2 Slot 120pin @ AD18  
PCI3 Slot 120pin @ AD19

IDE1 40pin  
Up to Ultra ATA/100  
Two IDE Channel

Mic In  
Line Out  
Line In

Audio Codec  
ALC850

AC' 97 & Lan I/F

LPC bus

SATA1 7Pin  
SATA2 7pin  
SATA3 7Pin  
SATA4 7pin

BW : 150MB/s

intel  
FWH  
32pin PLCC

TPM 1.1

Super I/O  
W38627THF  
128pin PQFP

VIA 1394

10/100  
Lan

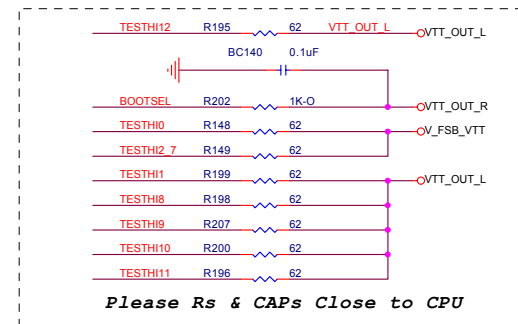
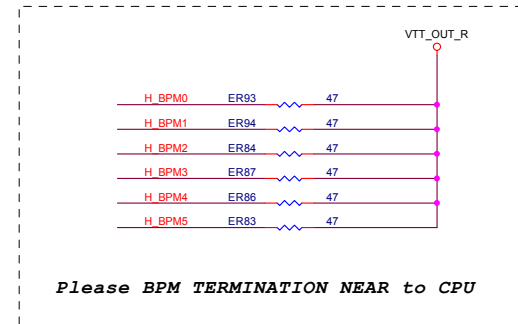
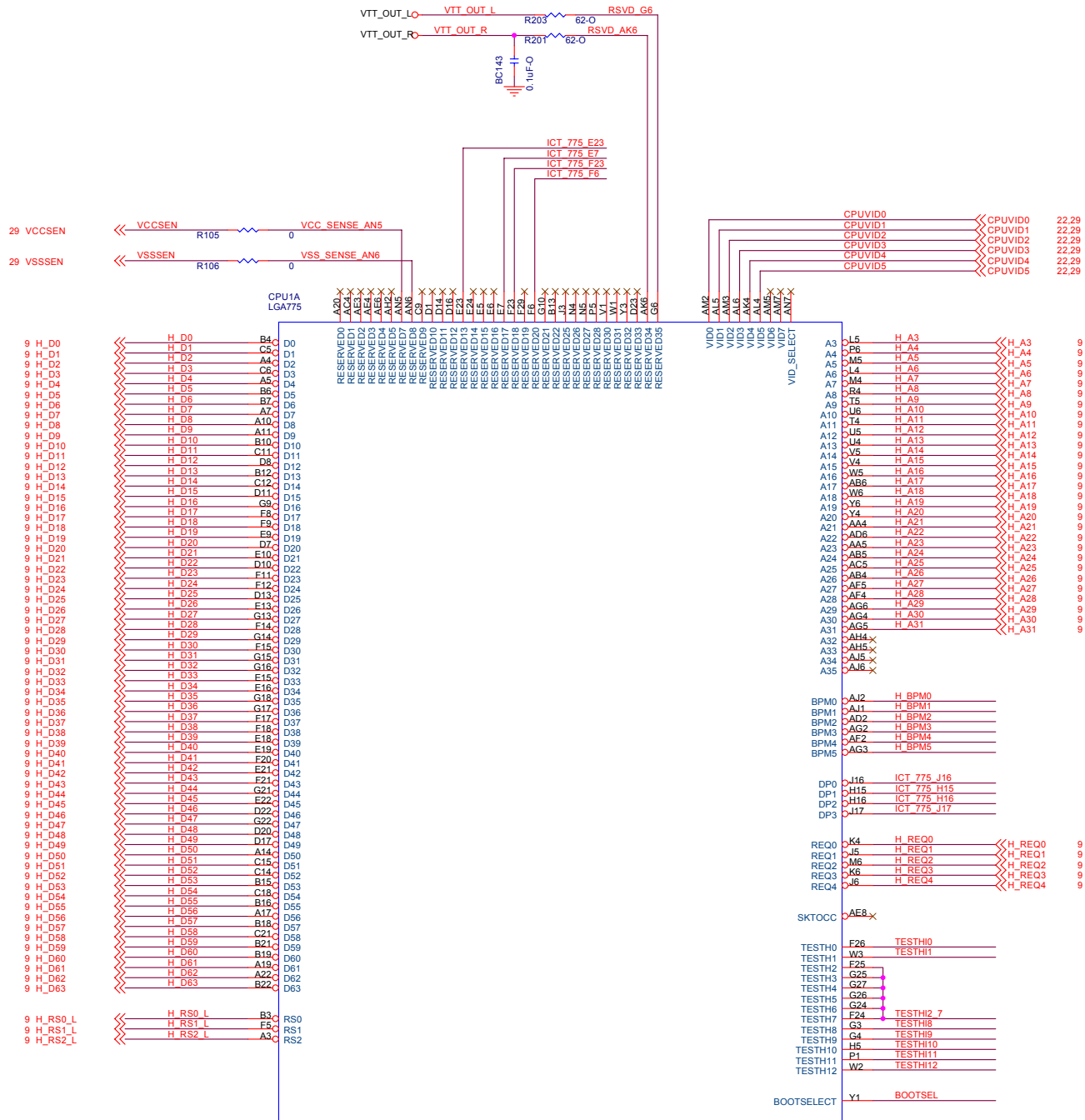
USBLAN  
RJ45

CONN/  
HEADER

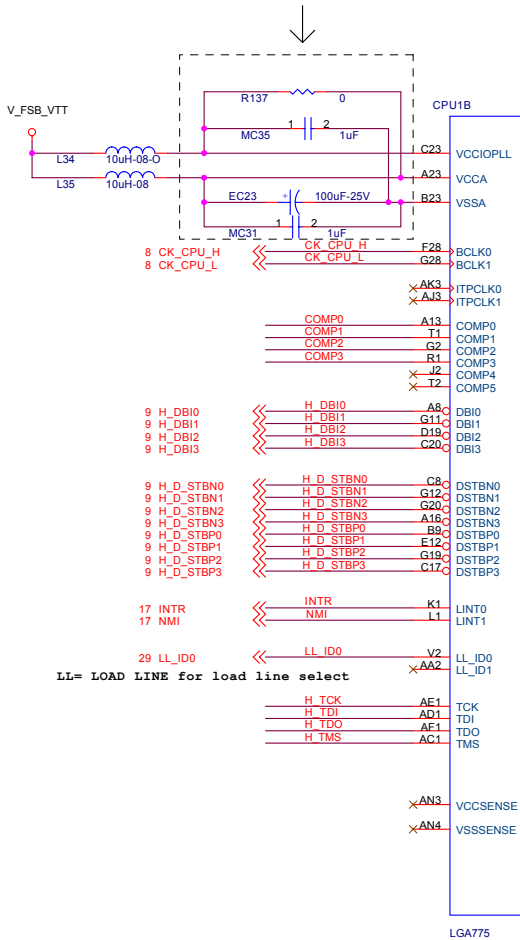


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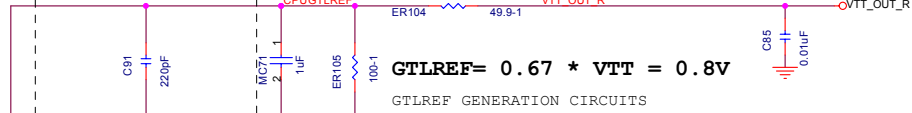
Title System Block Diagram		
Size B	Document Number 915GV-M5	Rev 1.0
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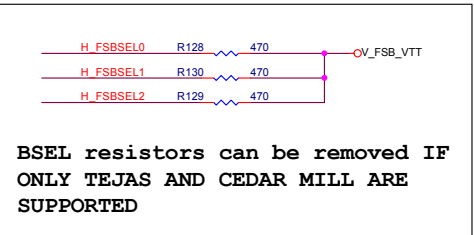
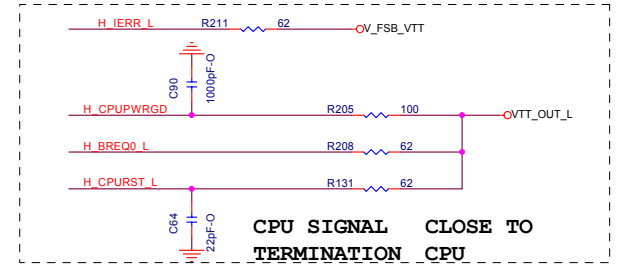
Place componets as close as possible to Processor socket  
trace width to cap must be no smaller than 12 Mils



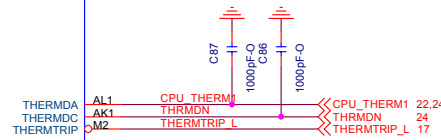
Close CPU H1 pin



GTLREF GENERATION CIRCUITS

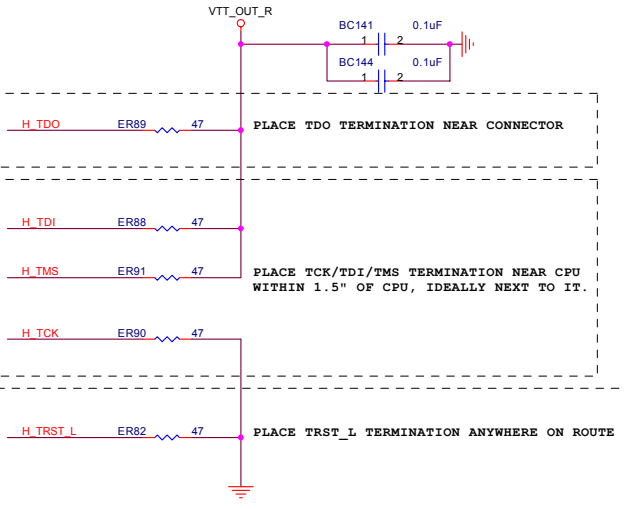


A20M	K3	A20M_L	17
ADS	D2	H_ADS_L	9
ADSTB0	R8	H_A_STB0	9
ADSTB1	AD5	H_A_STB1	9
AD3	X		
BNR	C2	H_BNR_L	9
BPRI	G8	H_BPRI_L	9
BRO	AC2	H_BREQ0_L	9
DBR	B2	H_DBSY_L	17,27
DEFER	G7	H_DEFER_L	9
DRDY	C1	H_DRDY_L	9
EDRDY	F2	H_EDRDY_L	9
FERR/PBE	R3	FERR_L	17
HIT	D4	H_HIT_L	9
HITM	E4	H_HITM_L	9
IERR	AB2	H_IERR_L	9
IGNNE	N2	IGNNE_L	17
INIT	C3	H_INIT_L	17
LOCK	C3	H_LOCK_L	9
MCERR	AB3	H_PCREQ_L	9
PC_REQ	G5	PCREQ_L	9
PROCHOT	AL2	PROCHOT_L	15
PWRGOOD	N1	H_CPUPWRGD	17
RESET	G23	H_CPURST_L	9
RSP	H4	SLP_L	17
SLP	CL2	SLP_L	17
SMT	P2	SMI_L	17
STPCLK	M3	STPCLK_L	17
TRDY	CE3	H_TRDY_L	9
TRST	AG1	H_TRST_L	9

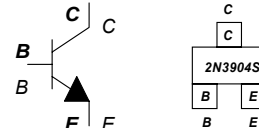
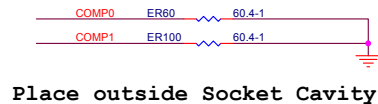


BSEL0	G29	H_FSBSEL0	8,9
BSEL1	H30	H_FSBSEL1	8,9
BSEL2	G30	H_FSBSEL2	8,9

AP0	U2	ICT 775 U2	
AP1	U3	ICT 775 U3	



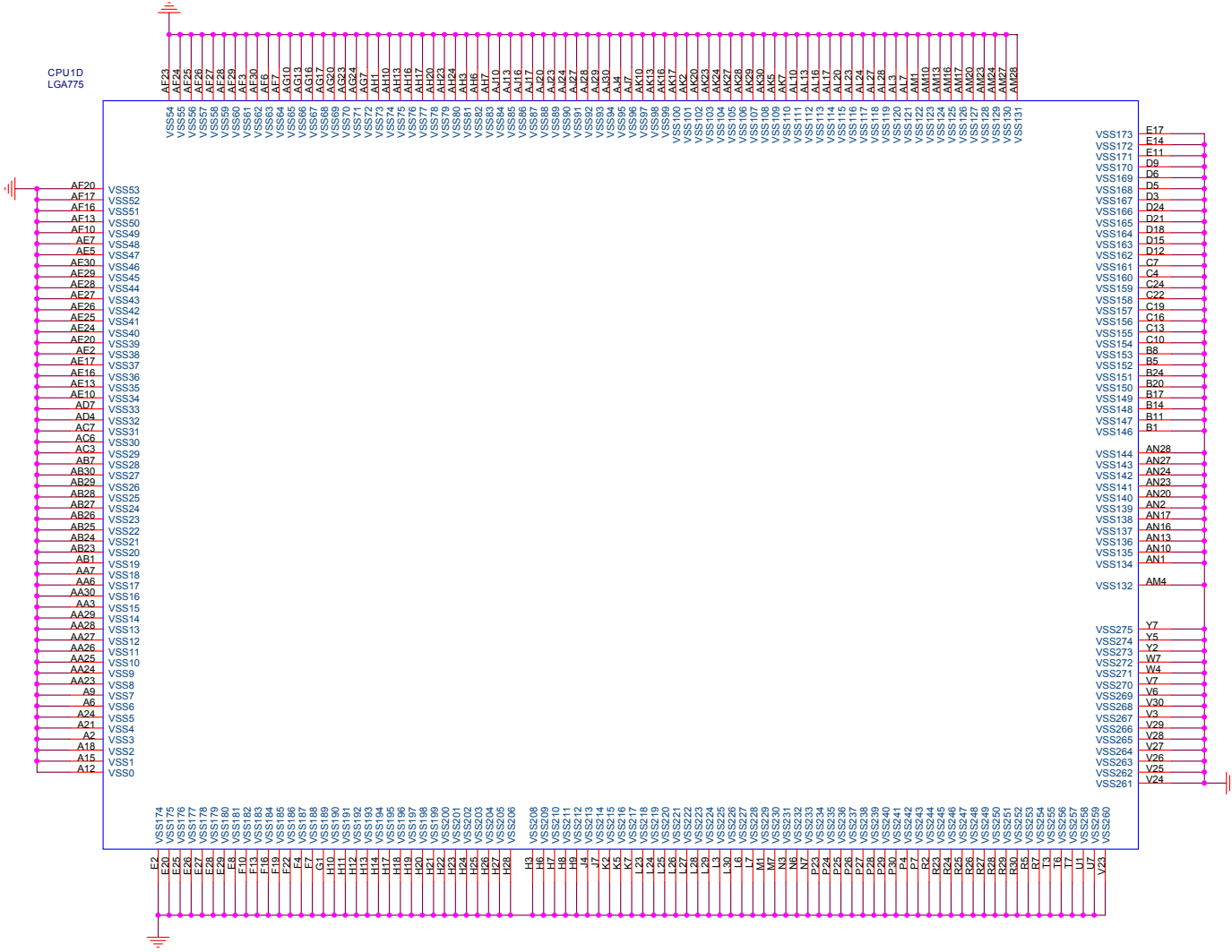
Layout need closed CPU

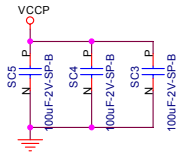
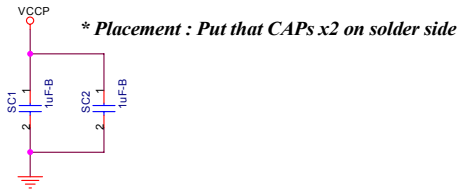
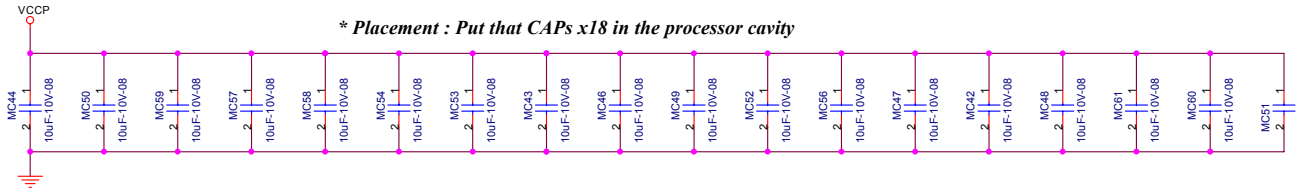




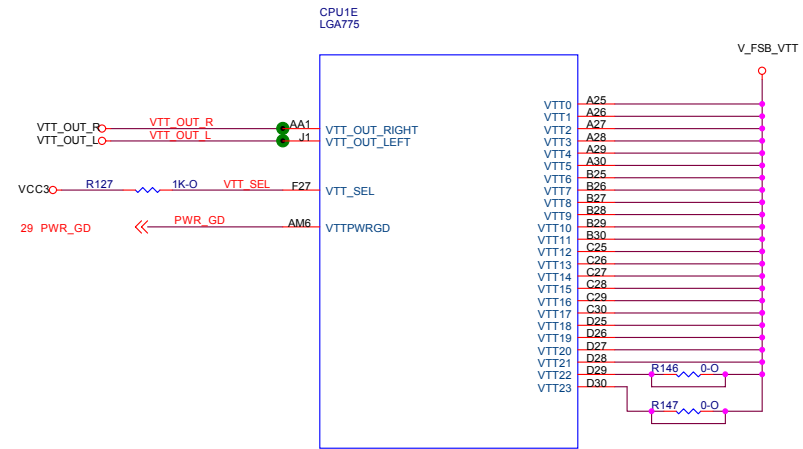
CPU1C  
LGA775

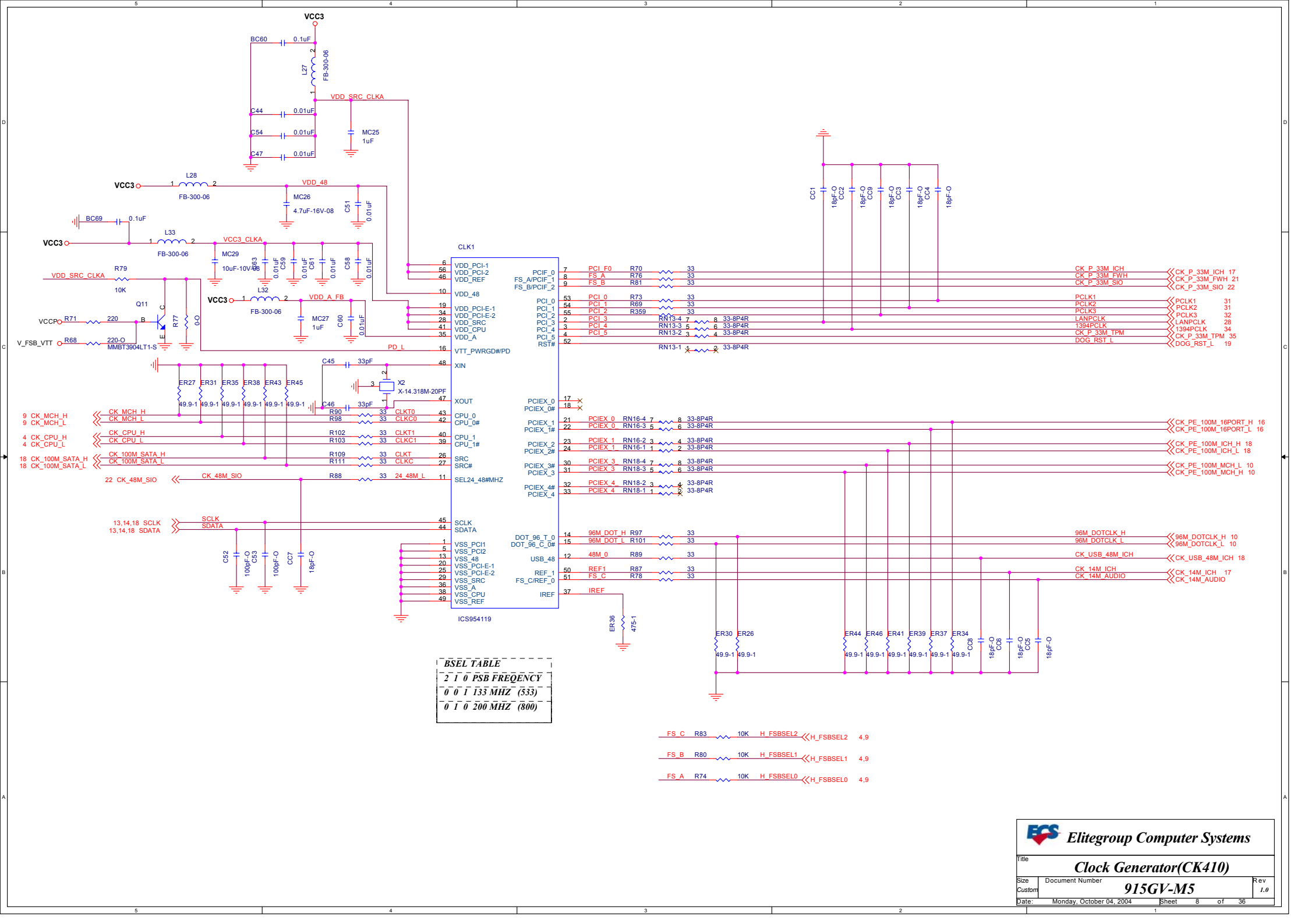
CPU1D  
LGA775





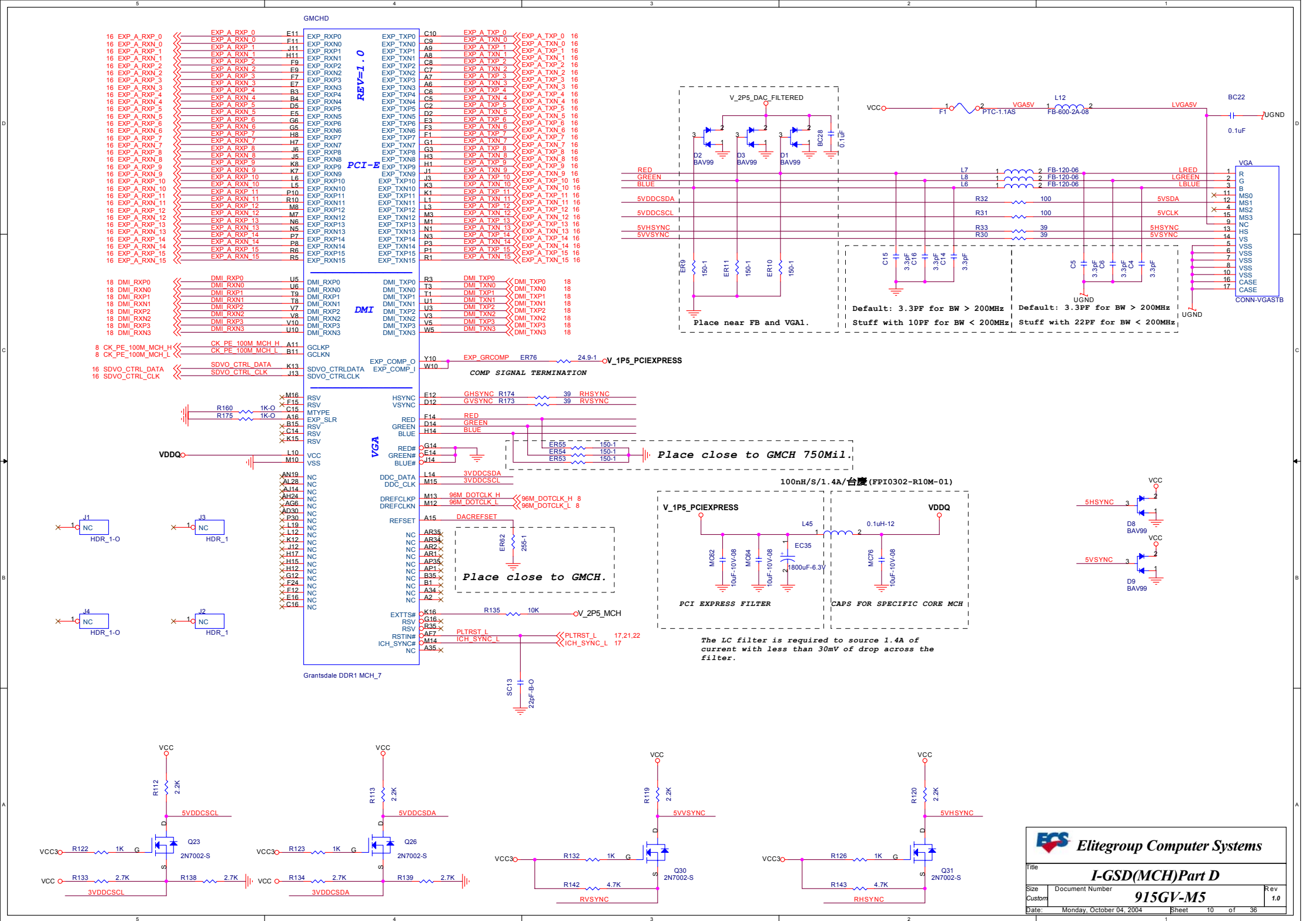
VTT\_SEL=0 for the Tejas processor














GMCHG

RSV

REV=1.0

GND

Grantsdale DDR1 MCH\_7

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Title

Schematic Change History

Size

Custom

Document Number

915GV-M5

Rev

1.0

Date:

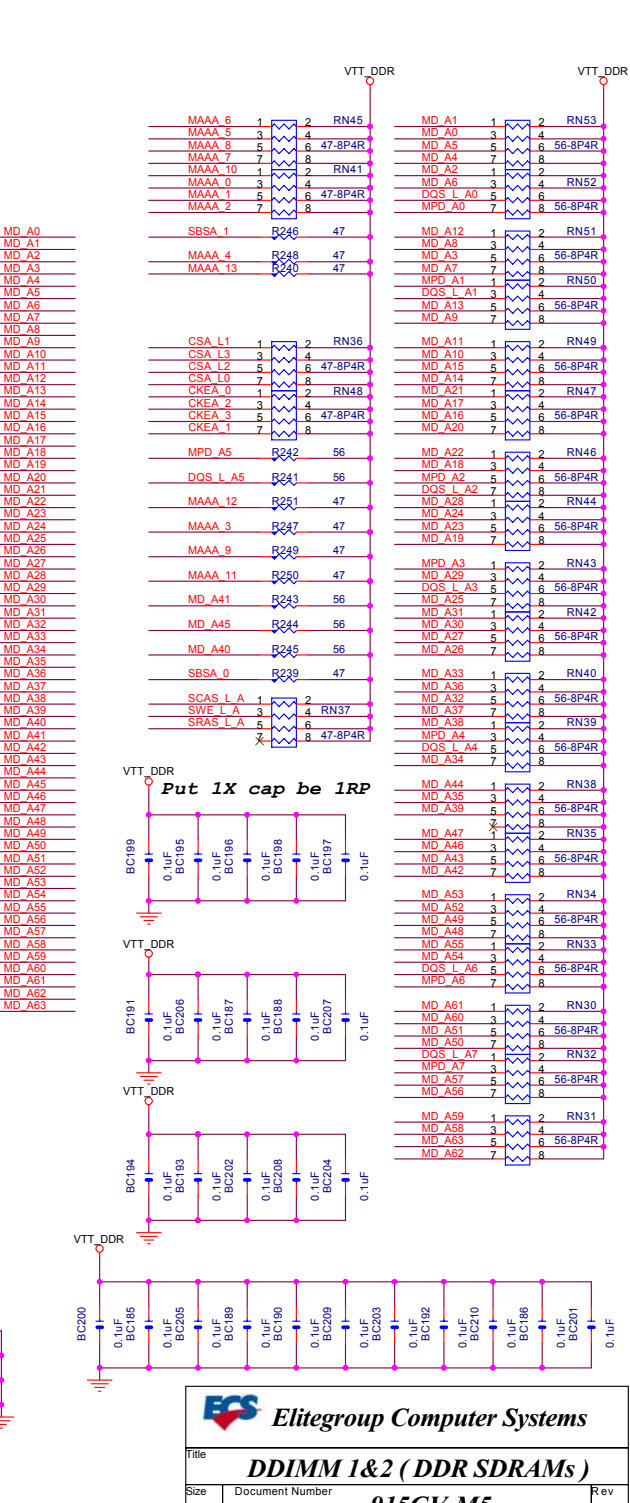
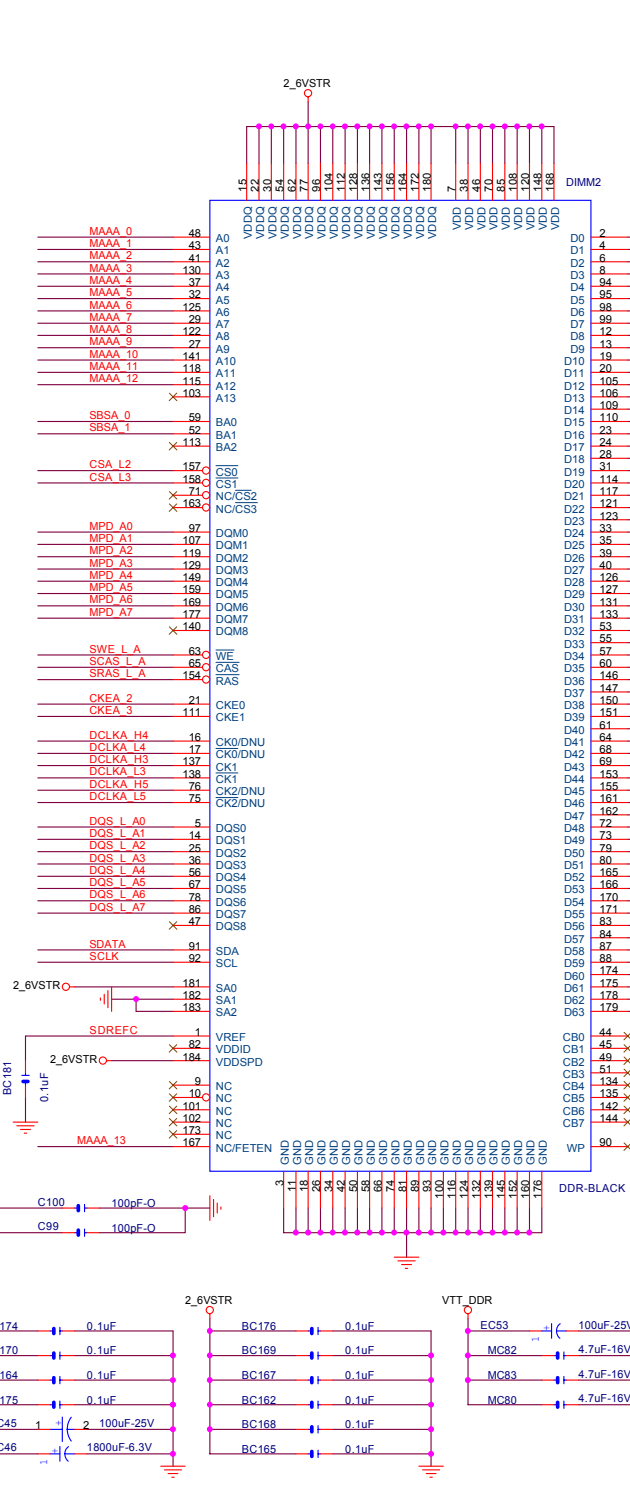
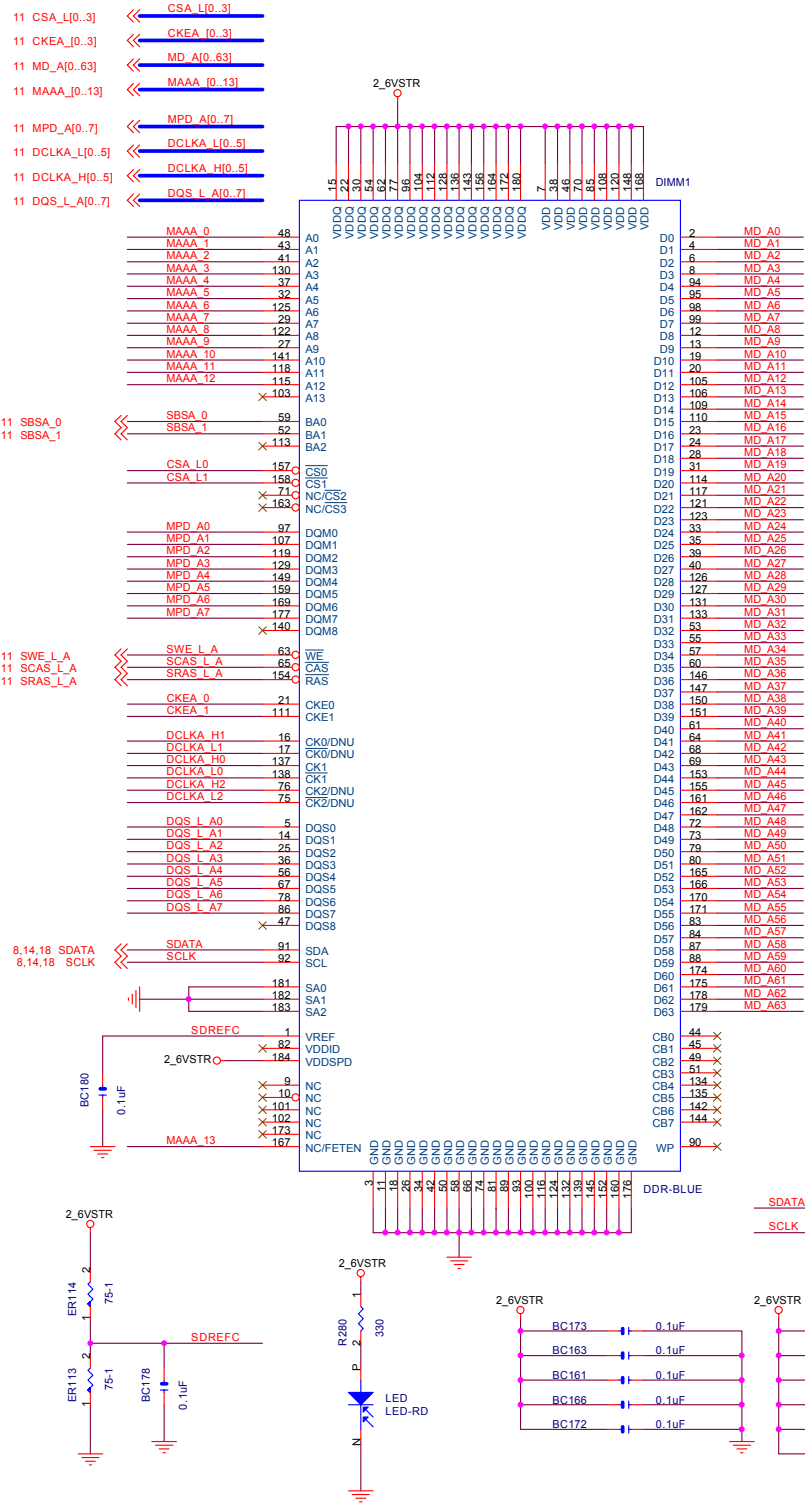
Monday, October 04, 2004

Sheet

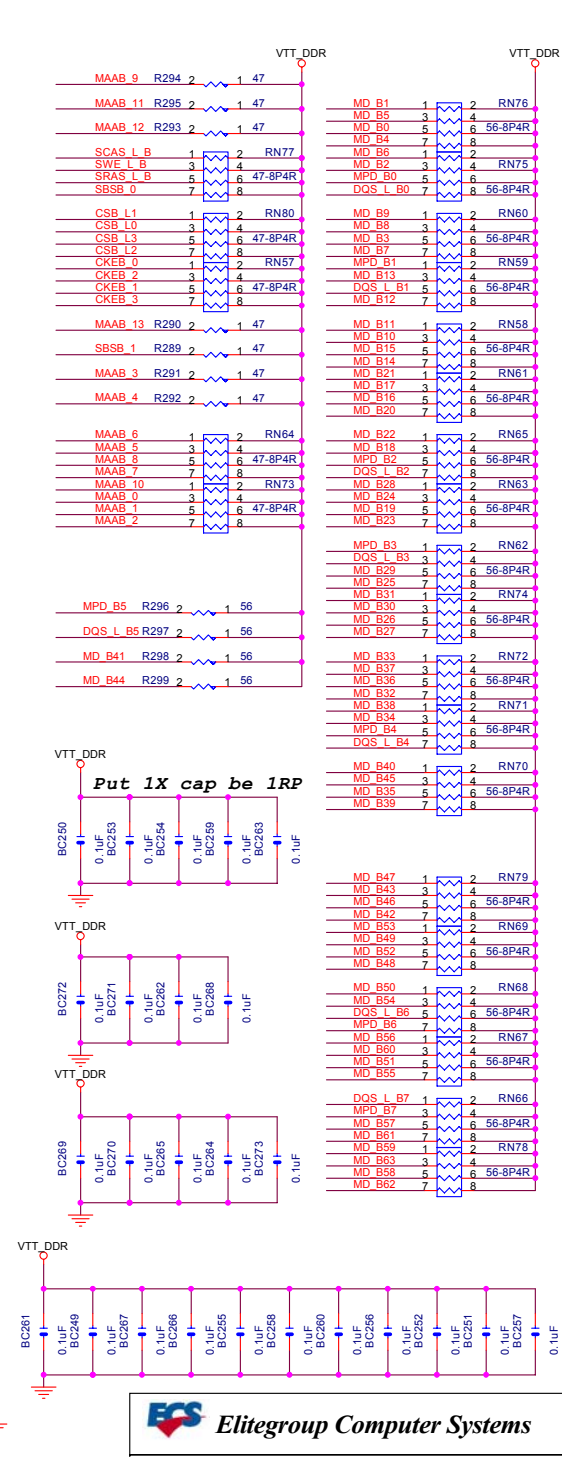
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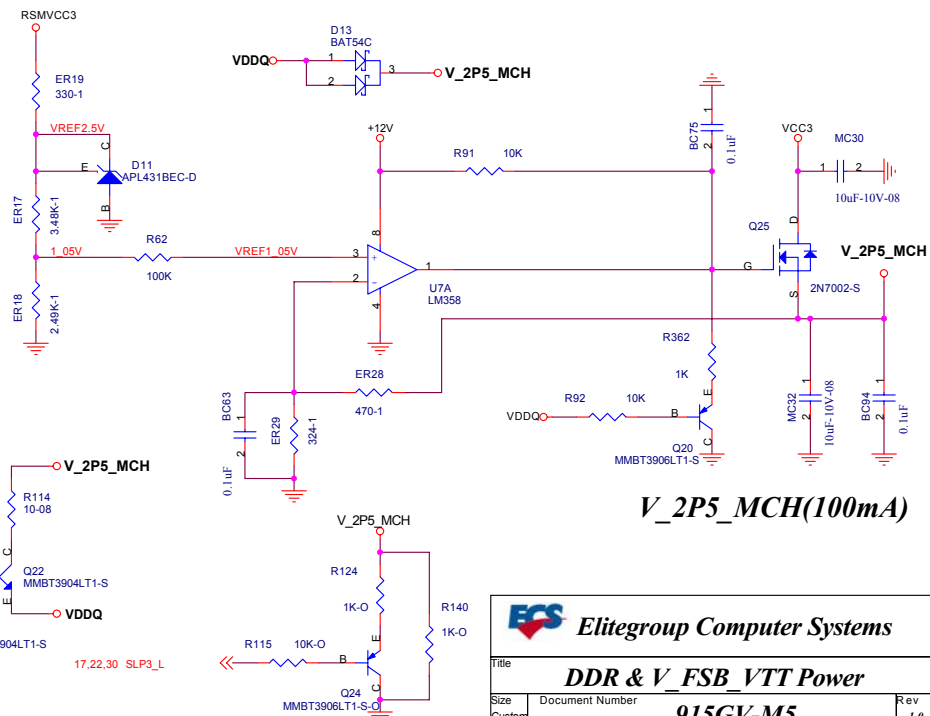
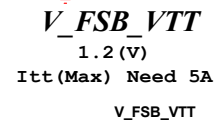
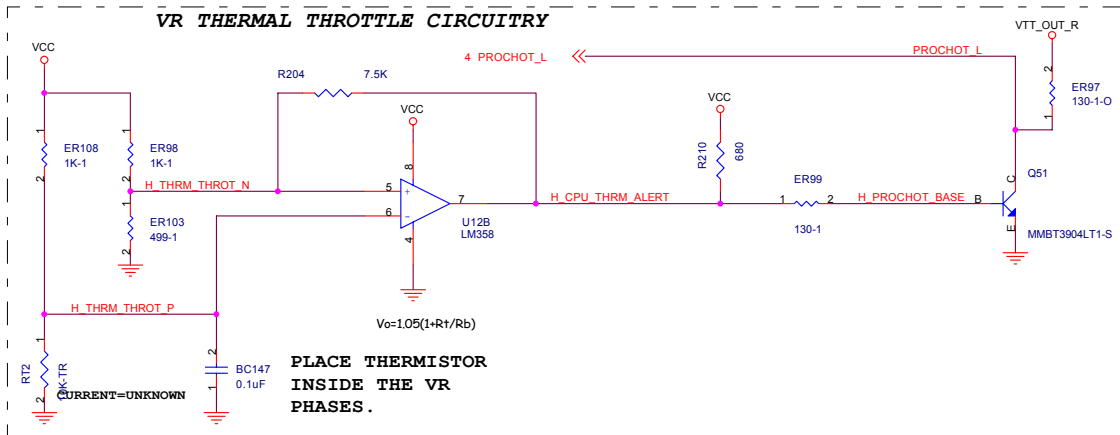
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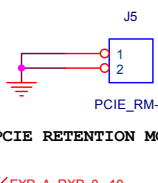
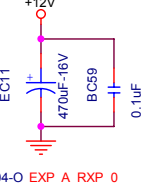
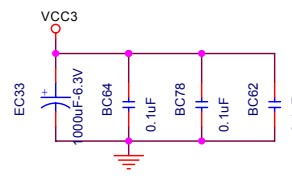
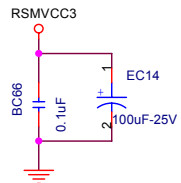
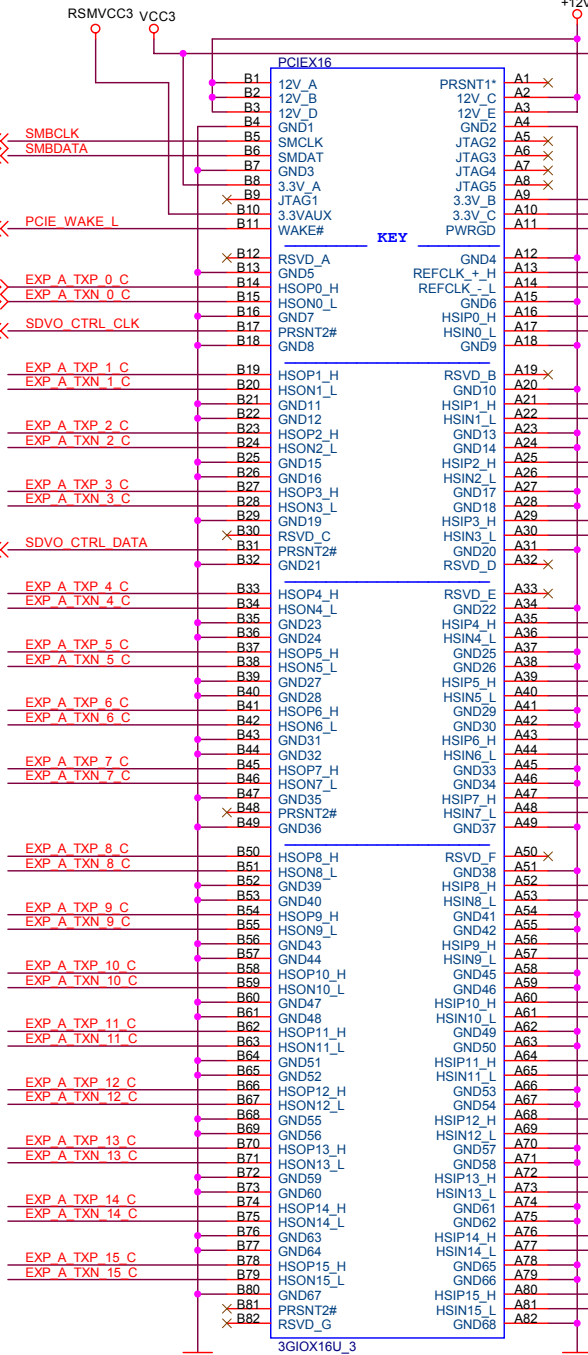


18,31,32 SMBCLK  
18,31,32 SMBDATA

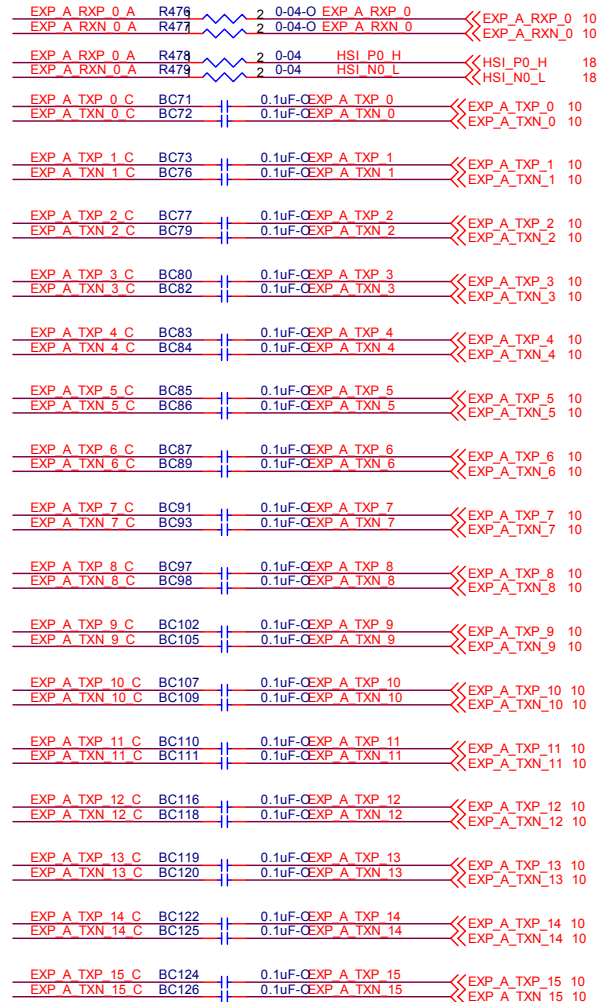
17 PCIE\_WAKE\_L


10 SDVO\_CTRL\_CLK

10 SDVO\_CTRL\_DATA



### PCIE RETENTION MODEL



**Elitegroup Computer Systems**

Title

**PCIE 16-PORT**

Size B

Document Number

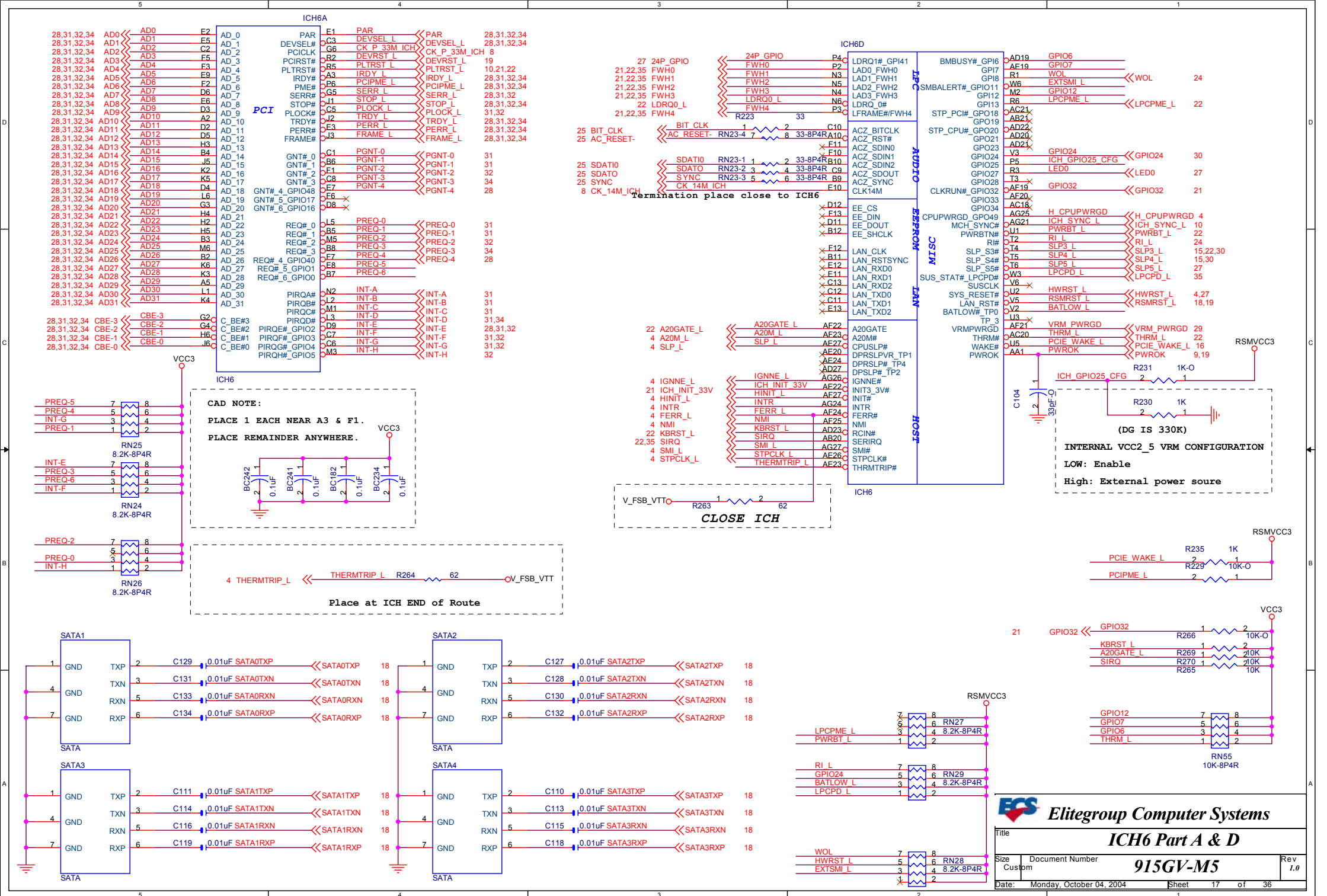
**915GV-M5**

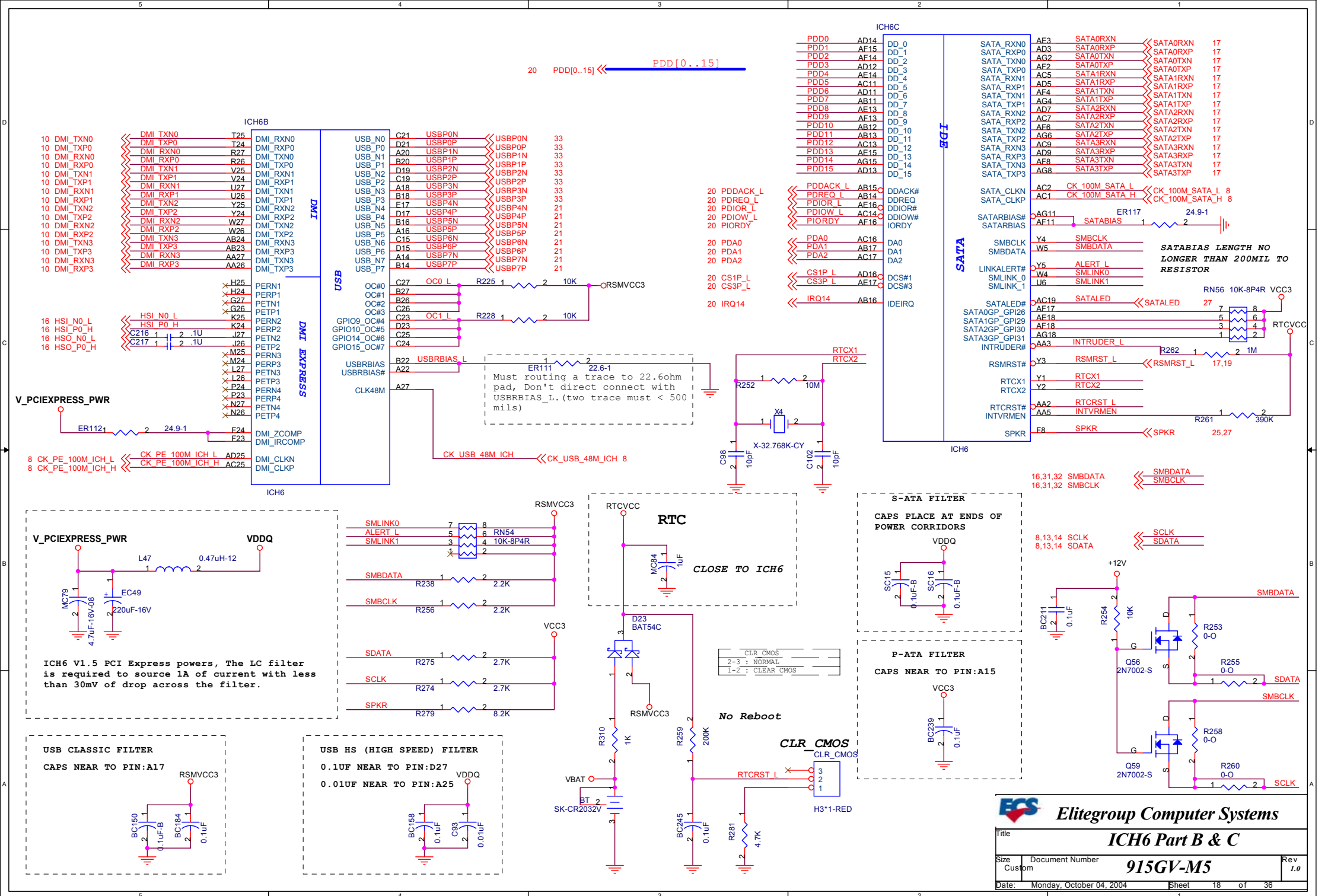
Rev  
1.0

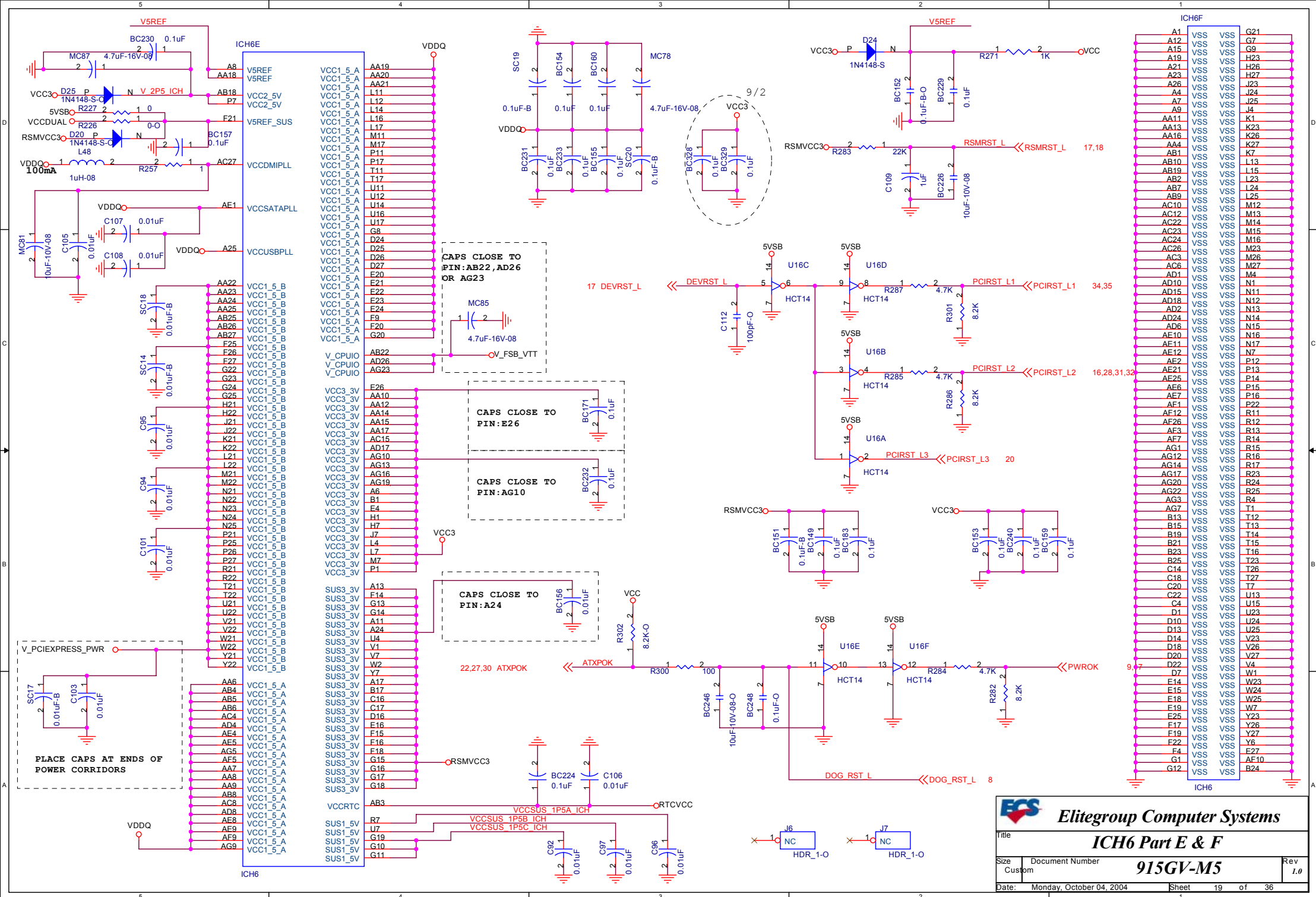
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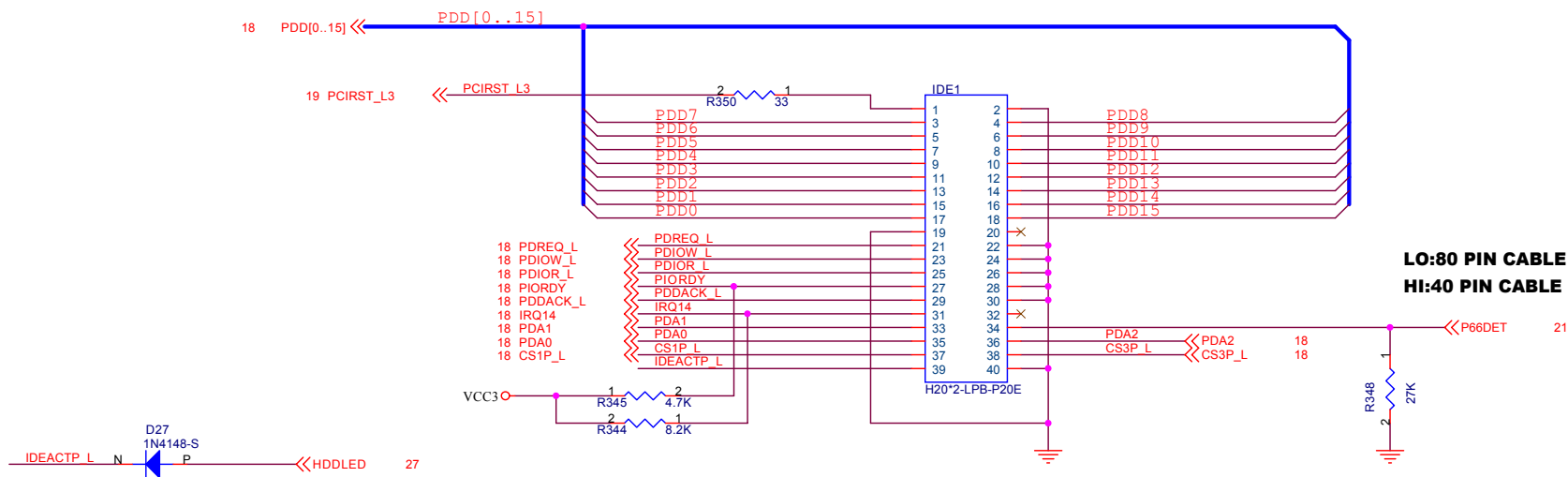
Sheet 16 of 36









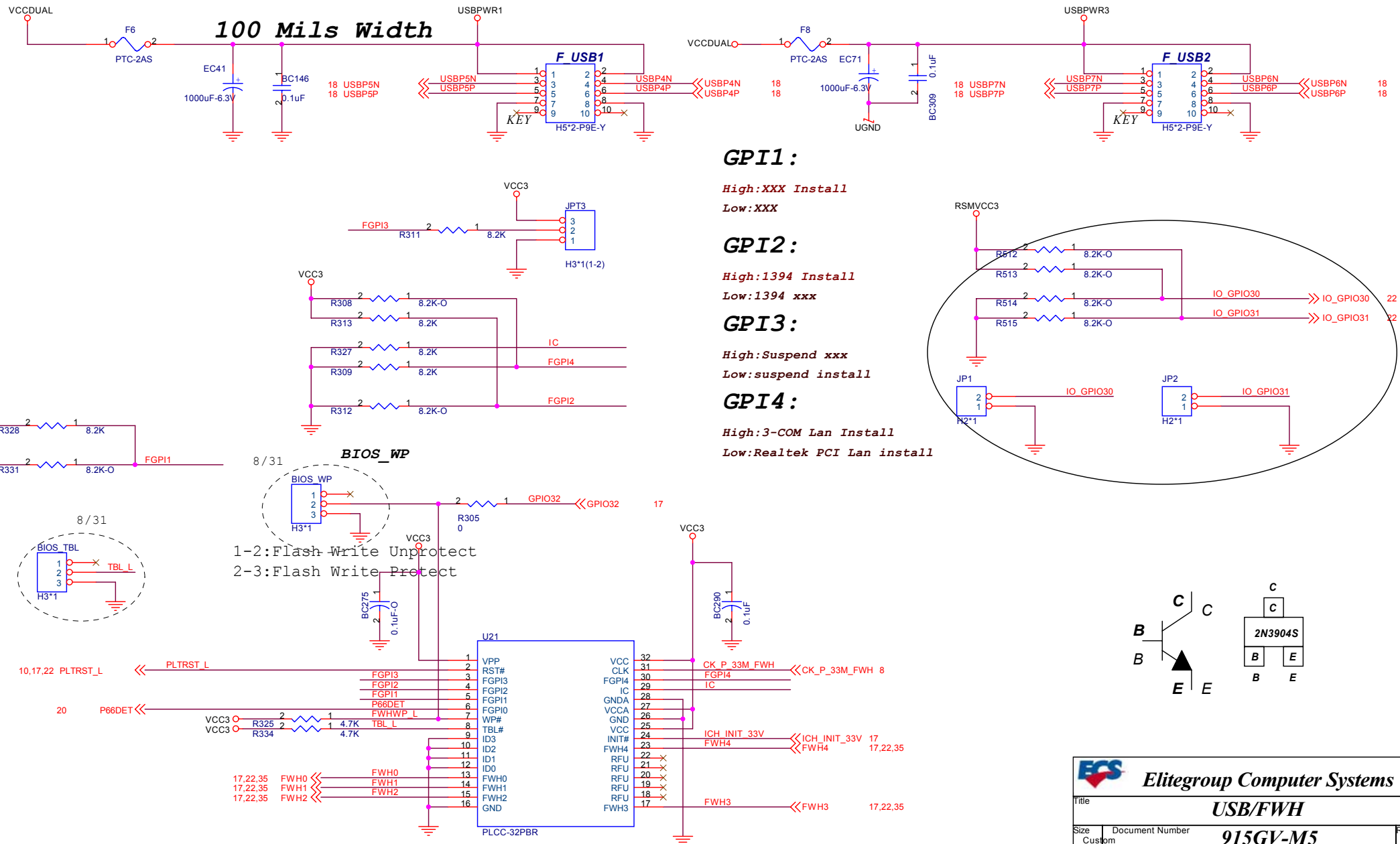


LO:80 PIN CABLE  
HI:40 PIN CABLE

# MAX TRACE LENGTH IS 8"

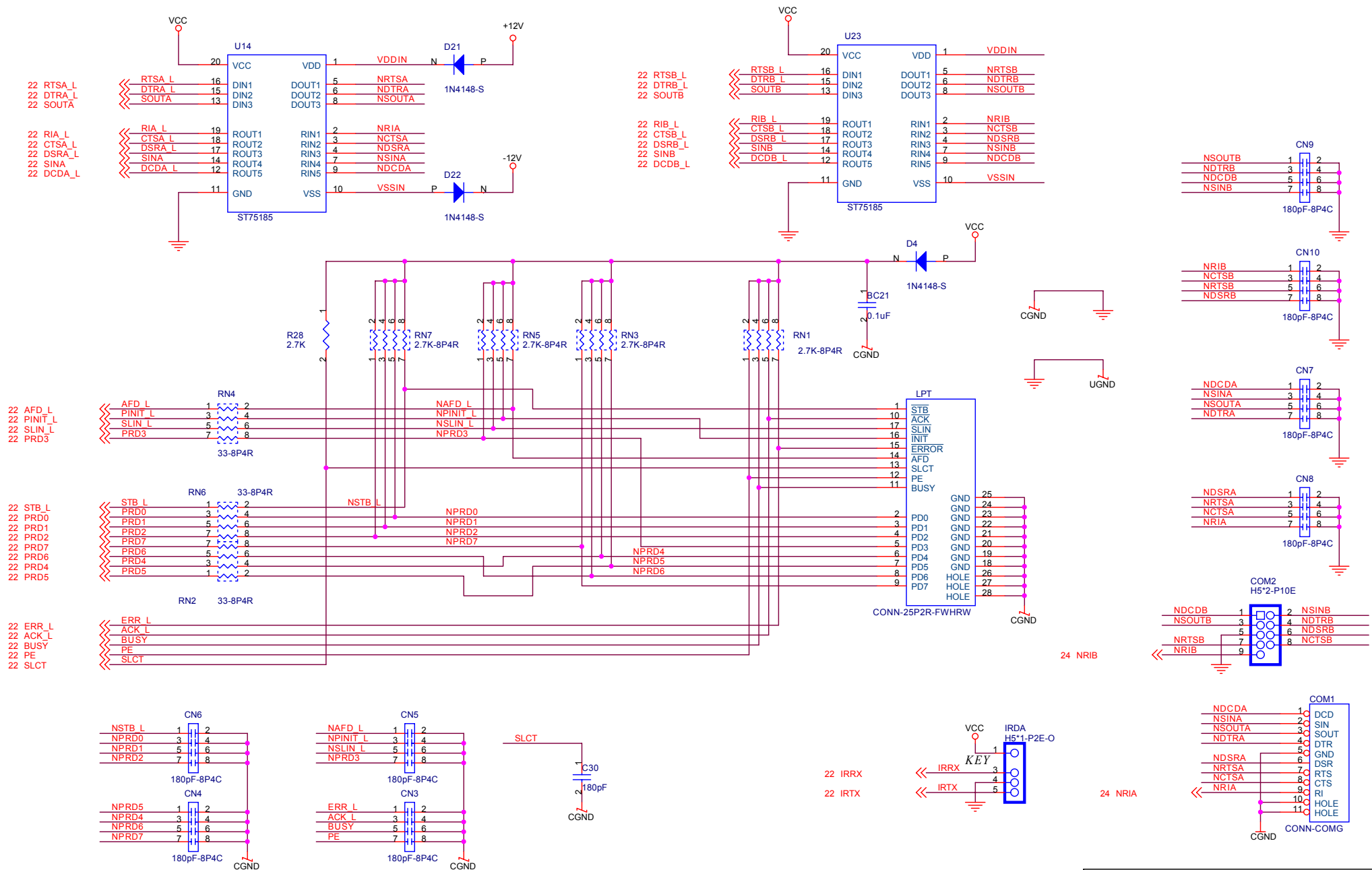
DATA LINES SHOULD BE MATCHED TO STROBES ( XDIOR\_L, XIORDY\_L) WITHIN +/- 250 MIL.,  
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/- 10MIL.

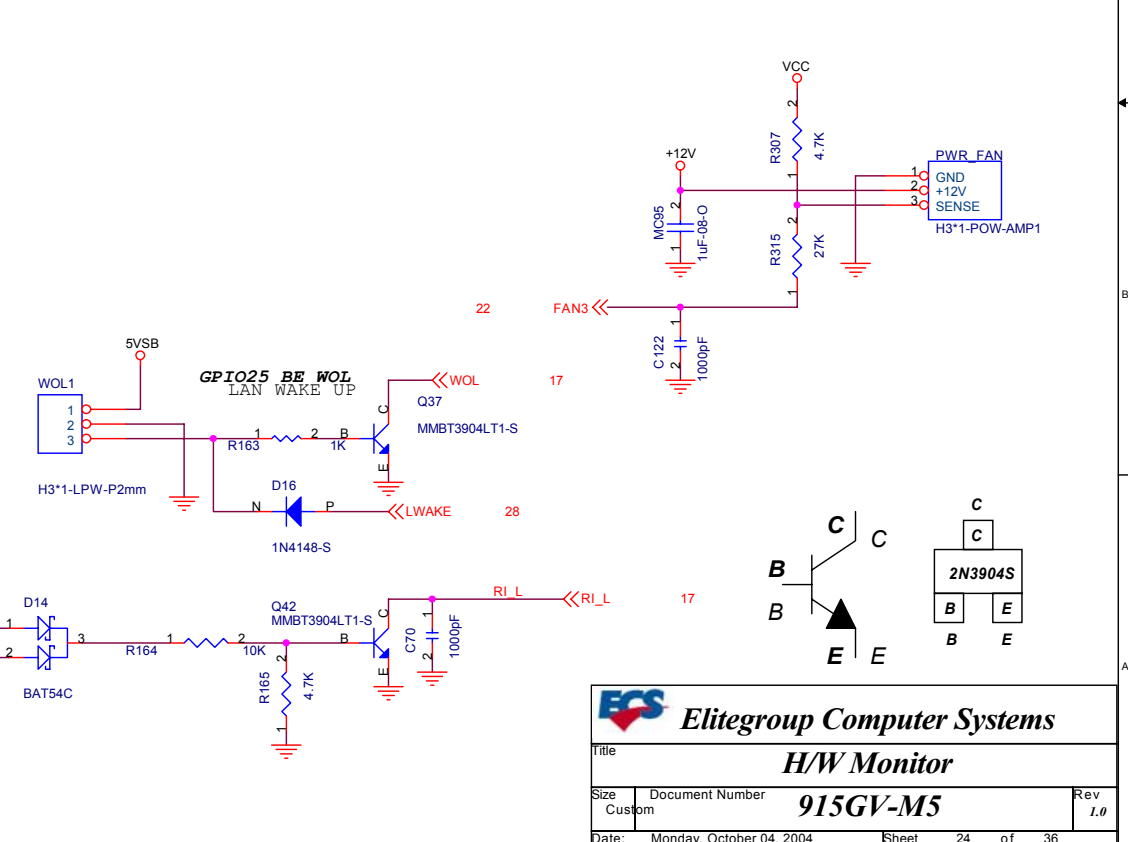
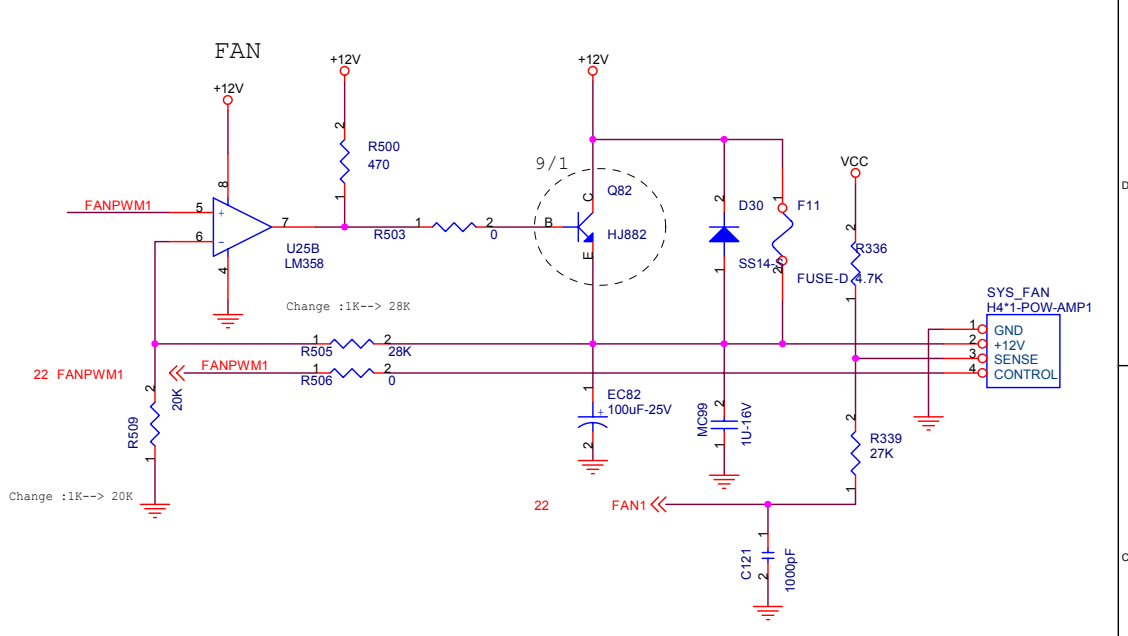
# USB PORT INTERFACE



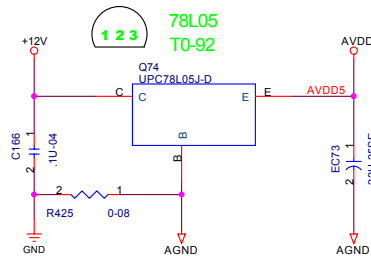
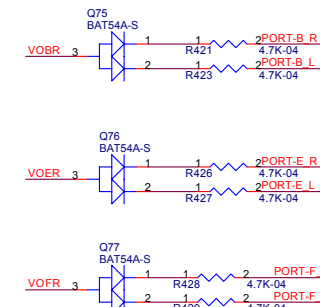




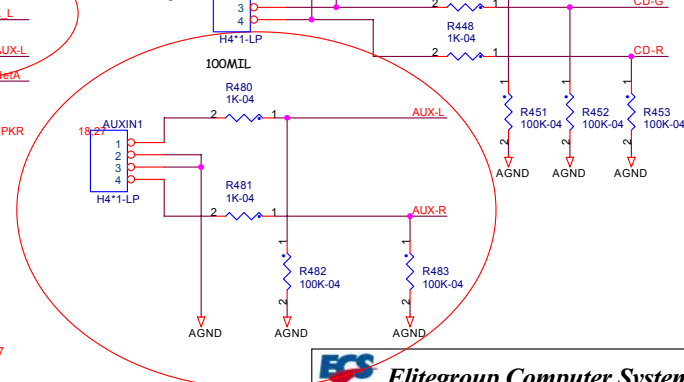
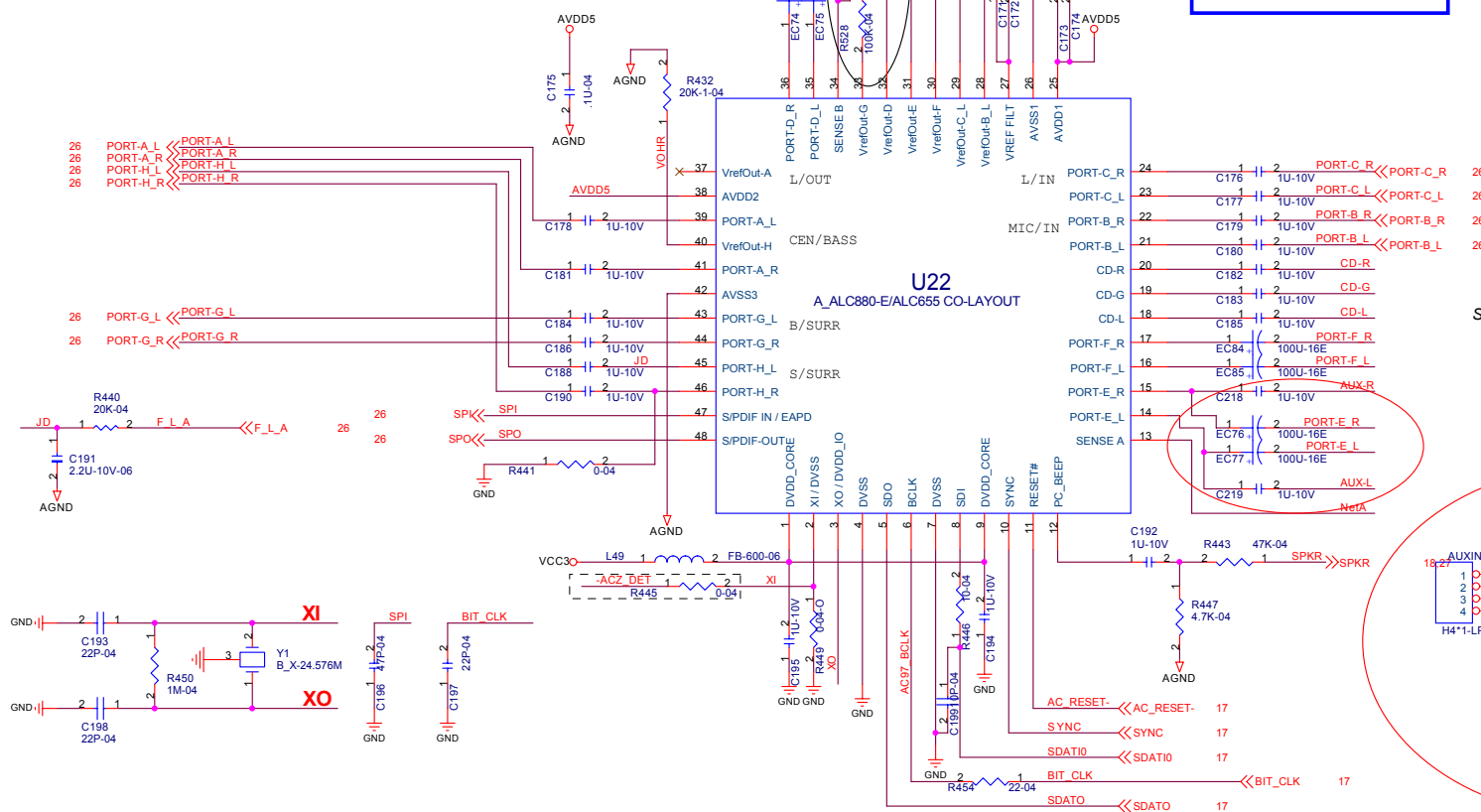




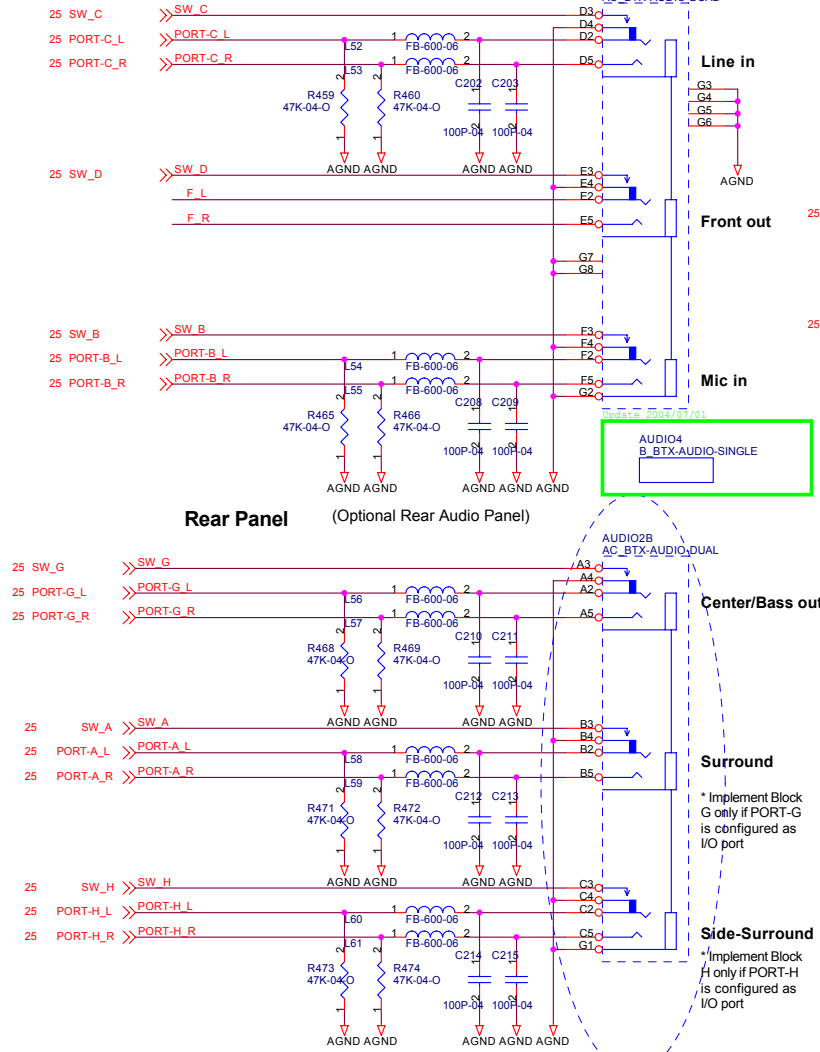


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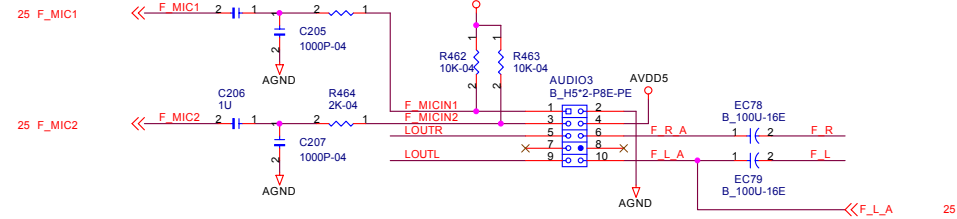
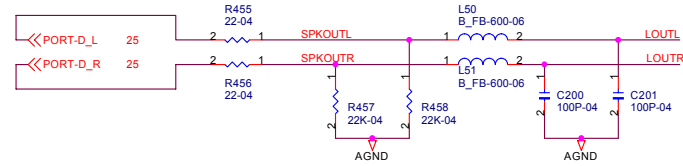
The diagram shows two multiplexers, NetA and NetB, connected to AVDD5. NetA has four inputs: R430 (1K-1.04-0), R431 (5.1K-1.04), R433 (10K-1.04), and R434 (20K-1.04). Its output is R435 (39.2K-1.04). NetB has four inputs: R436 (1K-1.04-0), R437 (5.1K-1.04), R438 (10K-1.04), and R439 (0-0). Its output is R440 (0-0). Both multiplexers are controlled by a 2-bit select signal from AVDD5, with SW\_D and SW\_C for NetA, and SW\_H and SenseB for NetB.



# Rear Panel Onboard Analog I/O

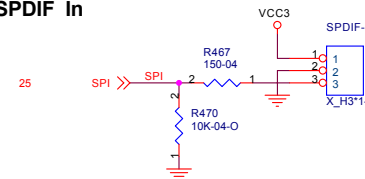


The schematic should consist with PINs define of I/O connector.

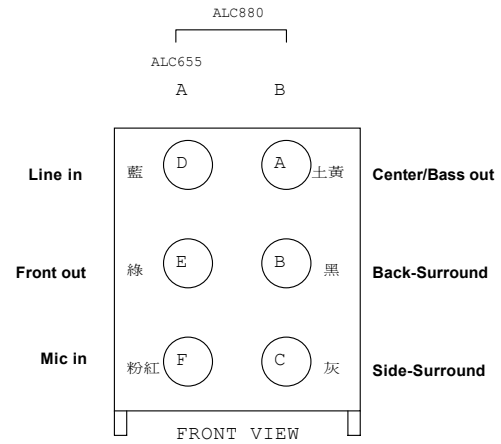
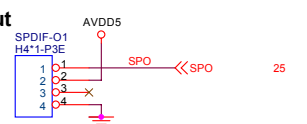


## SPDIF I/O

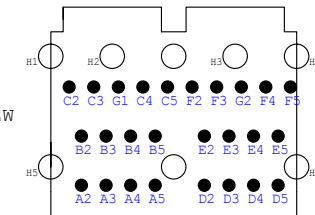
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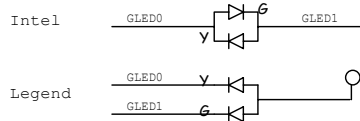
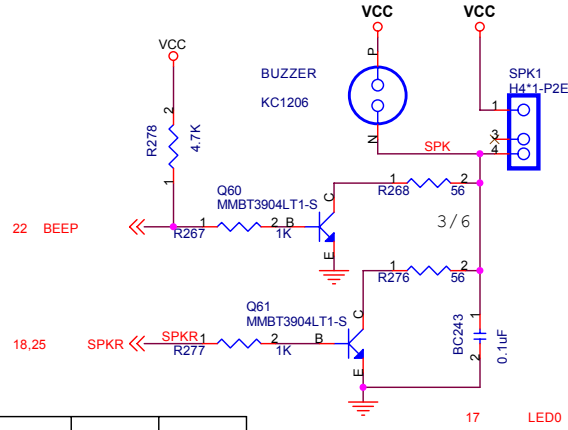
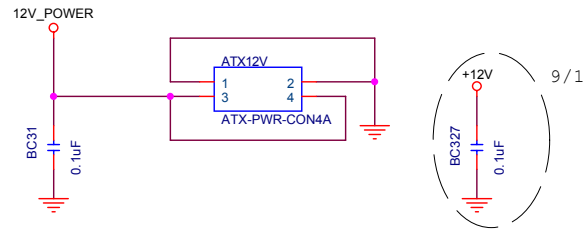
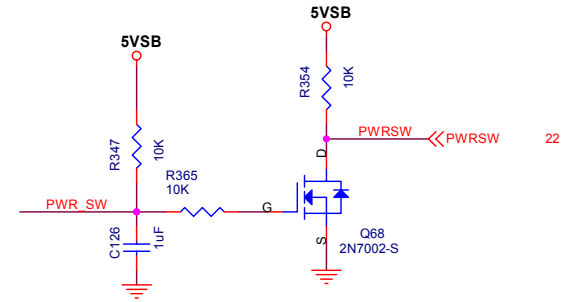
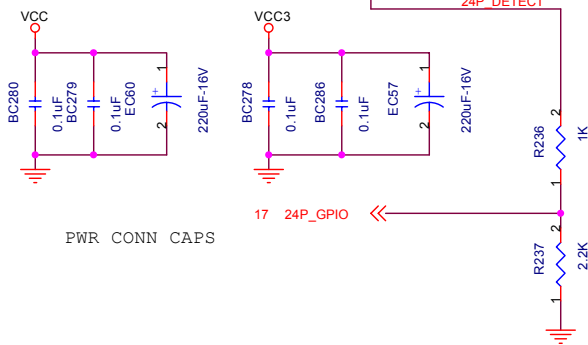
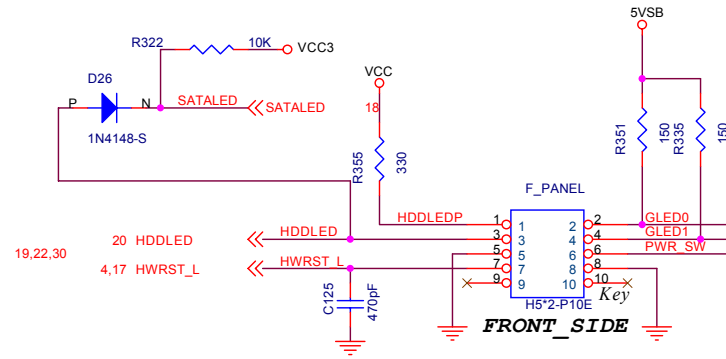
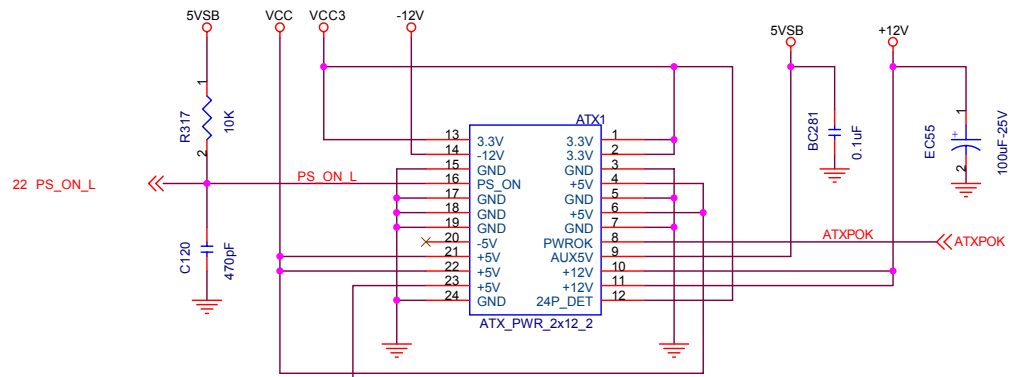


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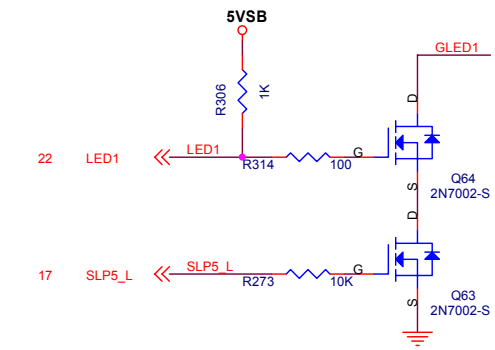
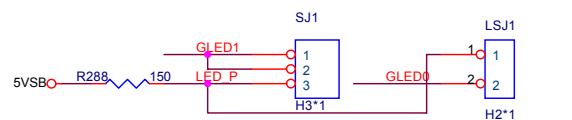


TOP VIEW





	S0	S1	S3	S4,S5
PANEL1 (4,2)	Green	G-blinking	Y-blinking	Dark
LPANEL1 (3,5,7)	Green	G-blinking	G-blinking	Dark
LSJ1 (1,2)	Dark	Dark	Light	Dark
SJ1 (1,3) (2,3)	Light	Blinking	Blinking	Dark
GLED0	HIGH	HIGH	LOW	HIGH
GLED1	LOW	SWITCH	SWITCH	HIGH



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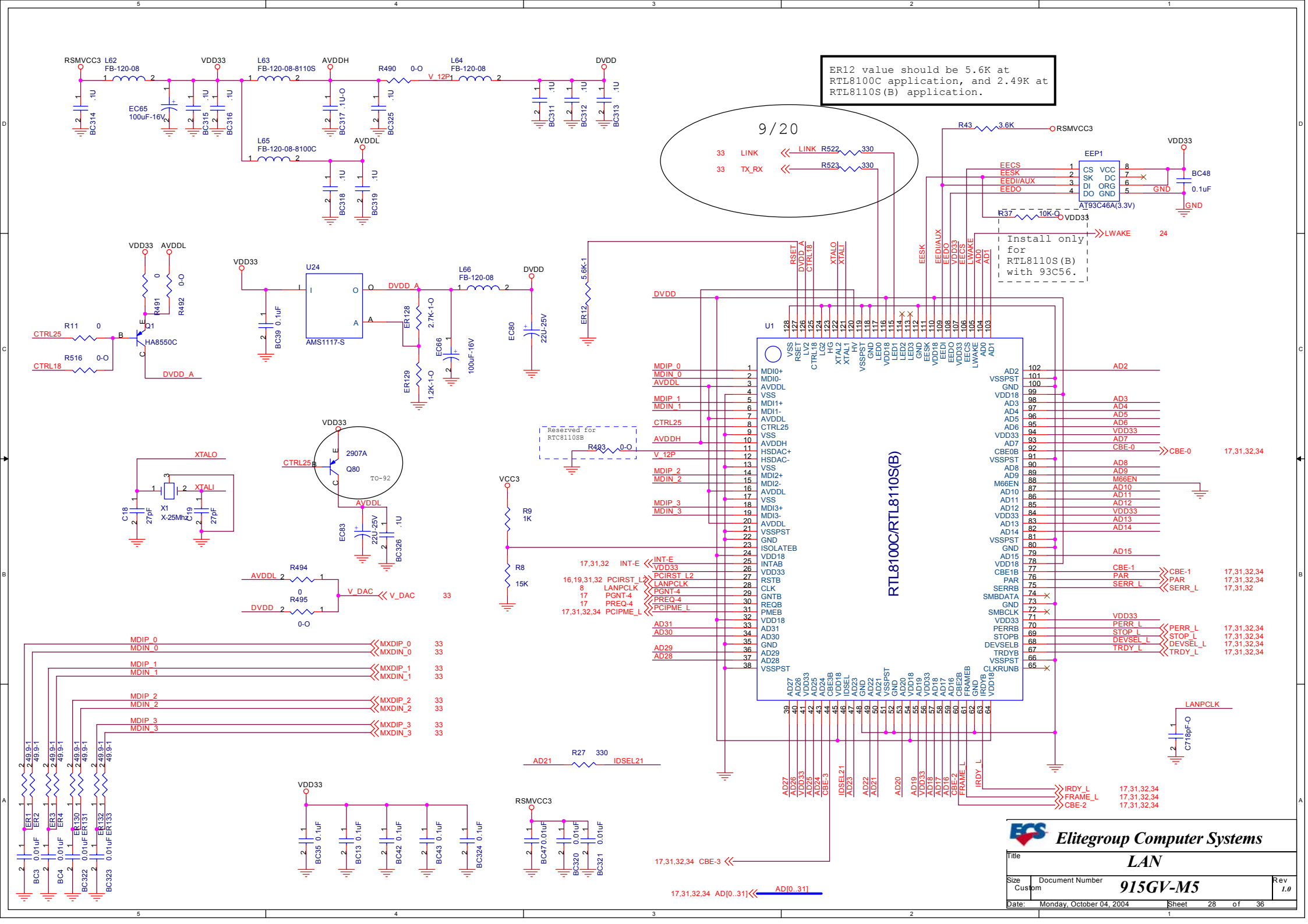
**ATX Power & Front Panel**

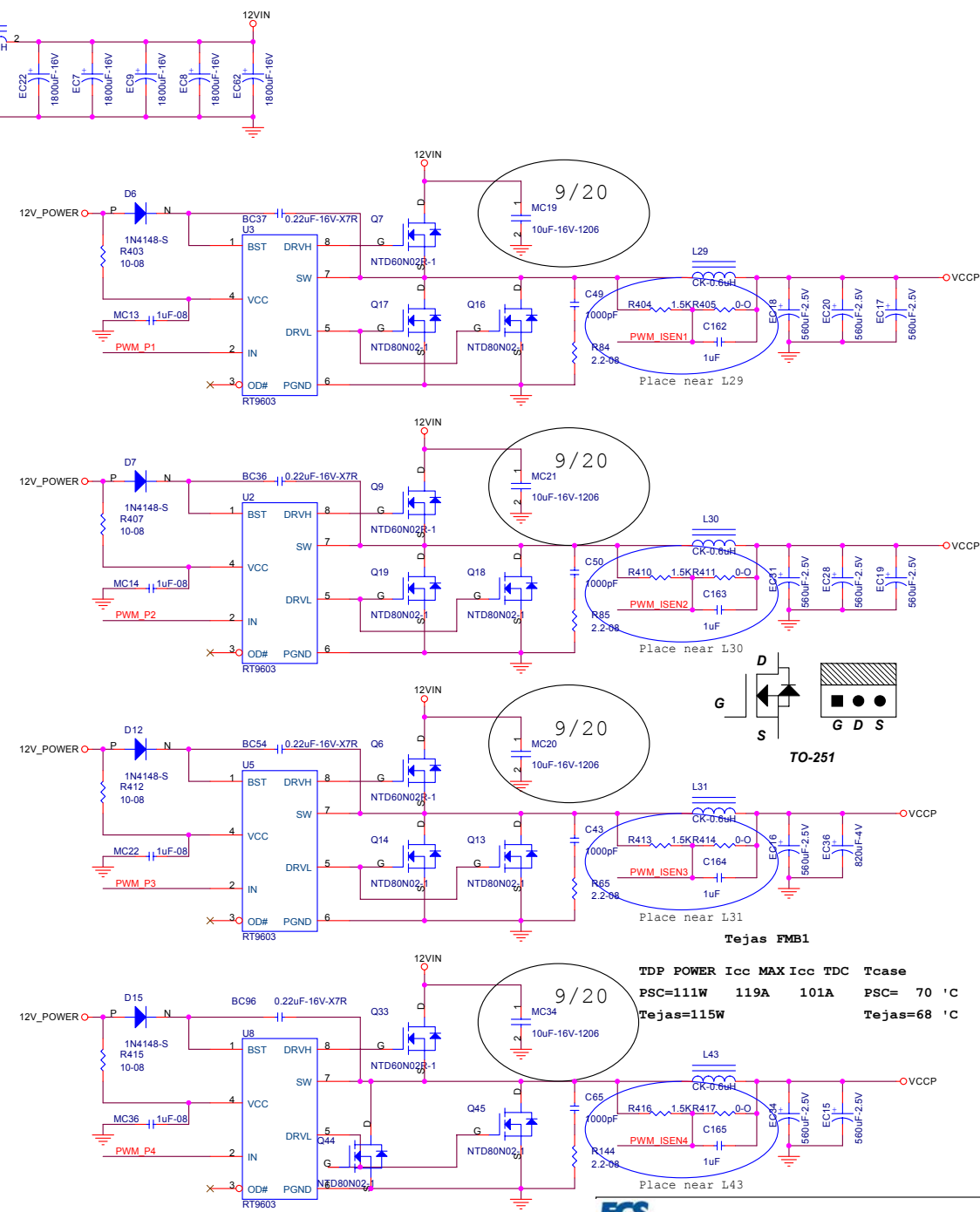
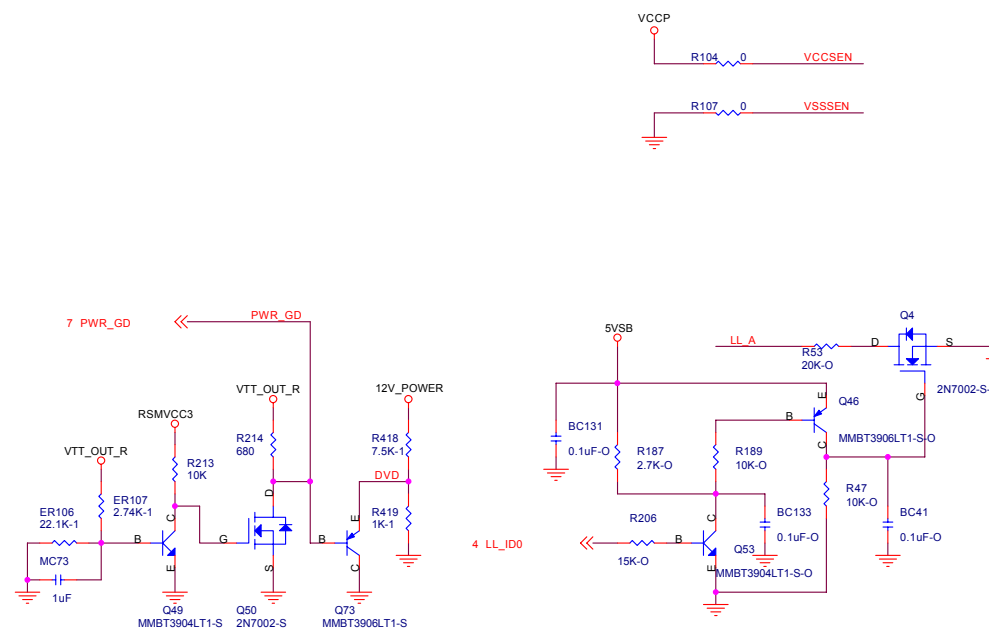
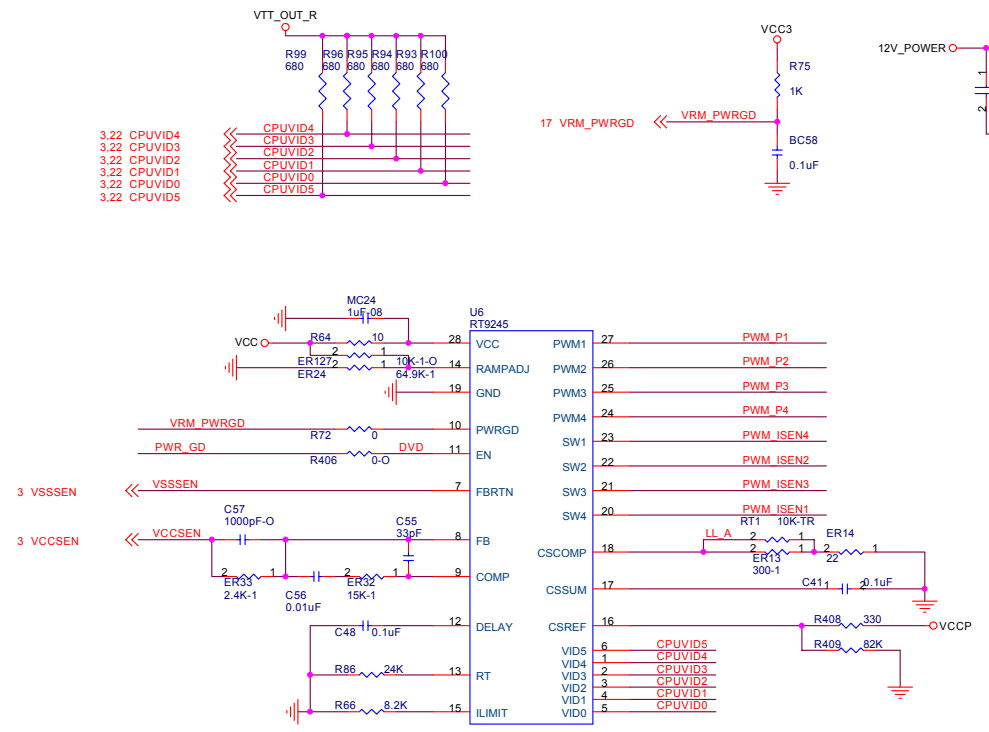
**915GV-M5**

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**Tejas FMB1**

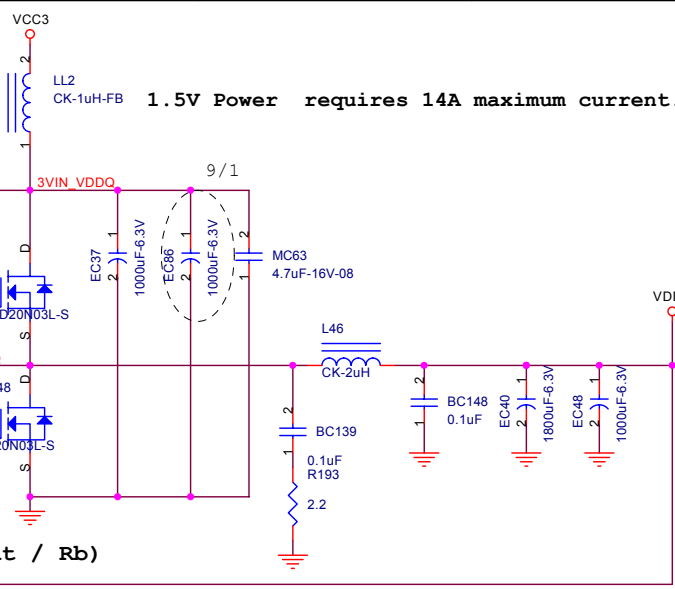
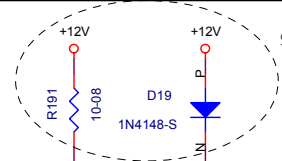
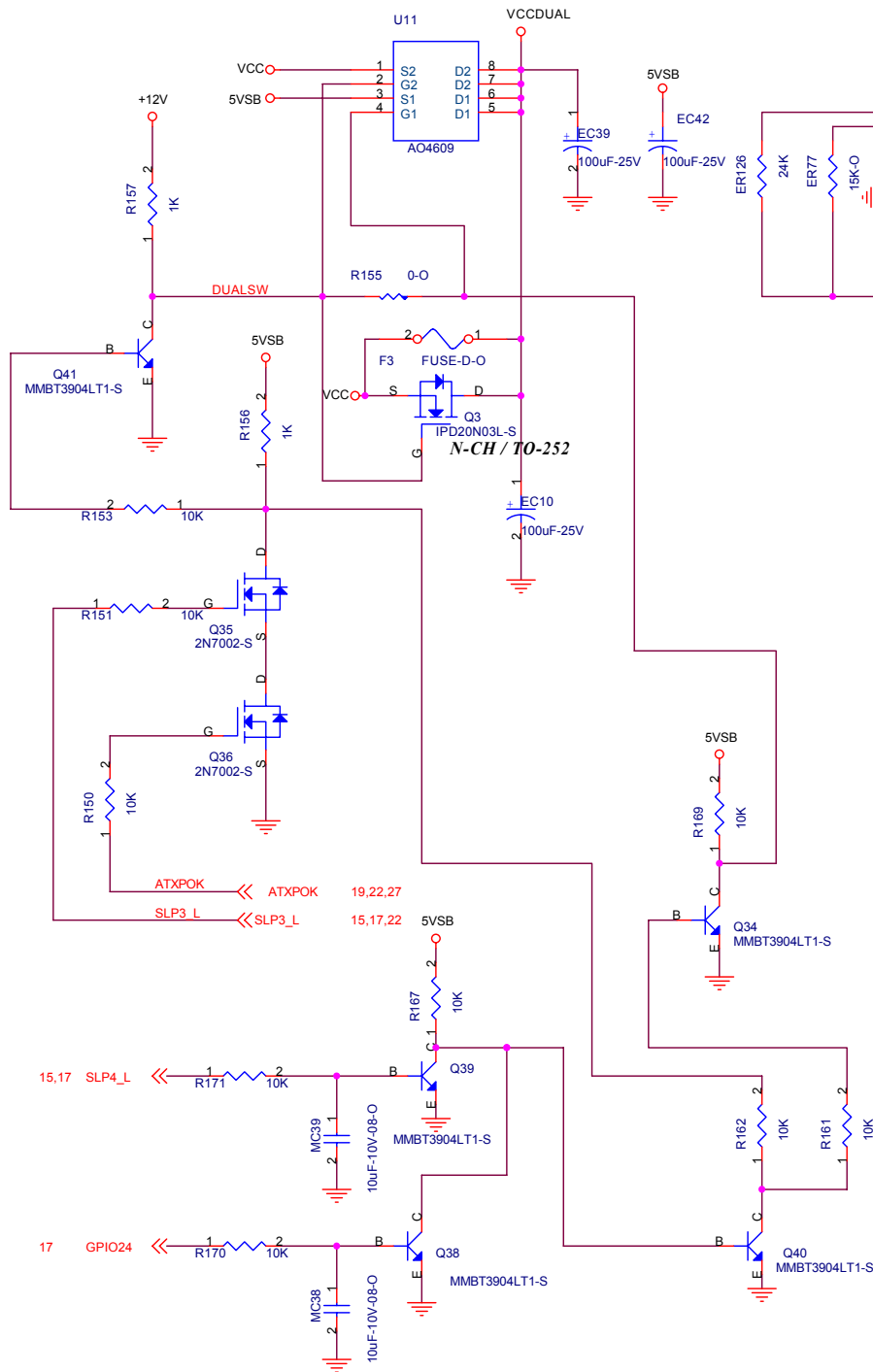
TDP	PSC	Icc	MAX Icc	TDC	Tcase
111W	119A	101A	PSC=	70 °C	
Tejas=115W				Tejas=68 °C	

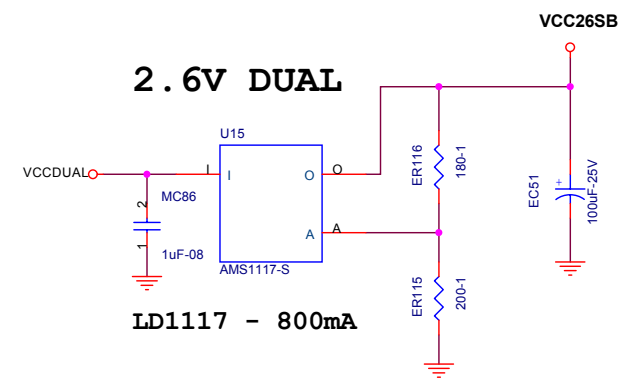
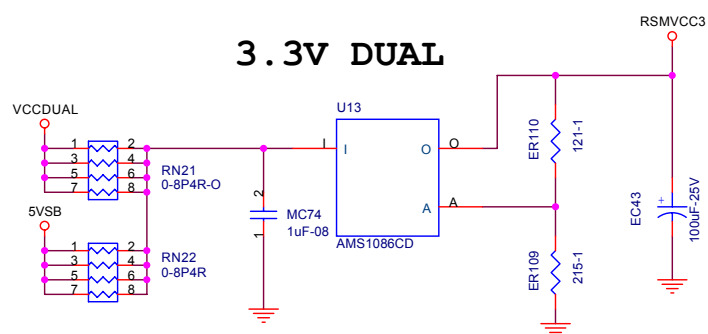
**Elitegroup Computer Systems**

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DUALSW << DUALSW 15



Signal Mode	GPIO24	VCCDUAL
S4/S5	0	0 (No Power)
S4/S5	1	1 (5VSB)



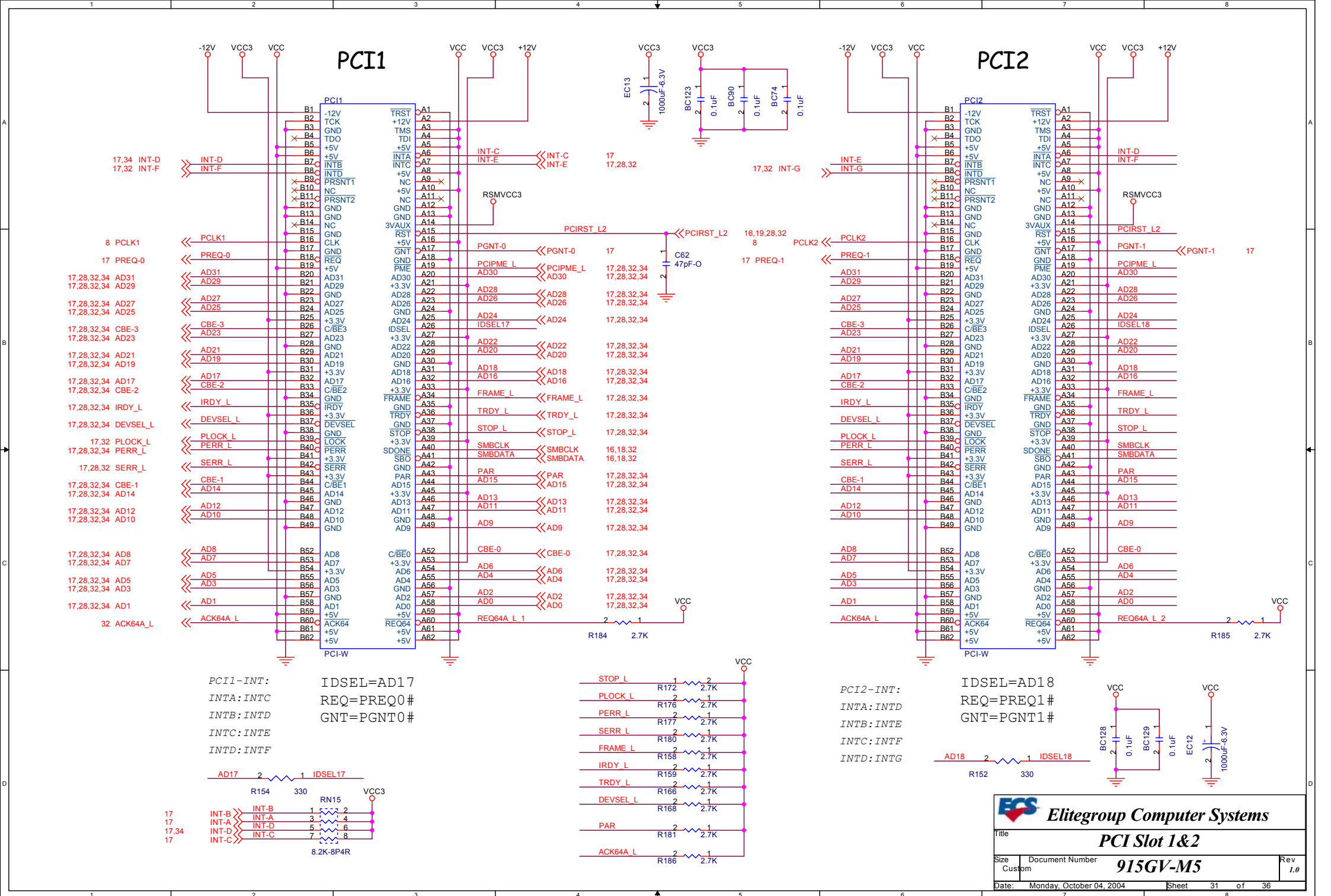
1.5V Power requires 14A maximum current.

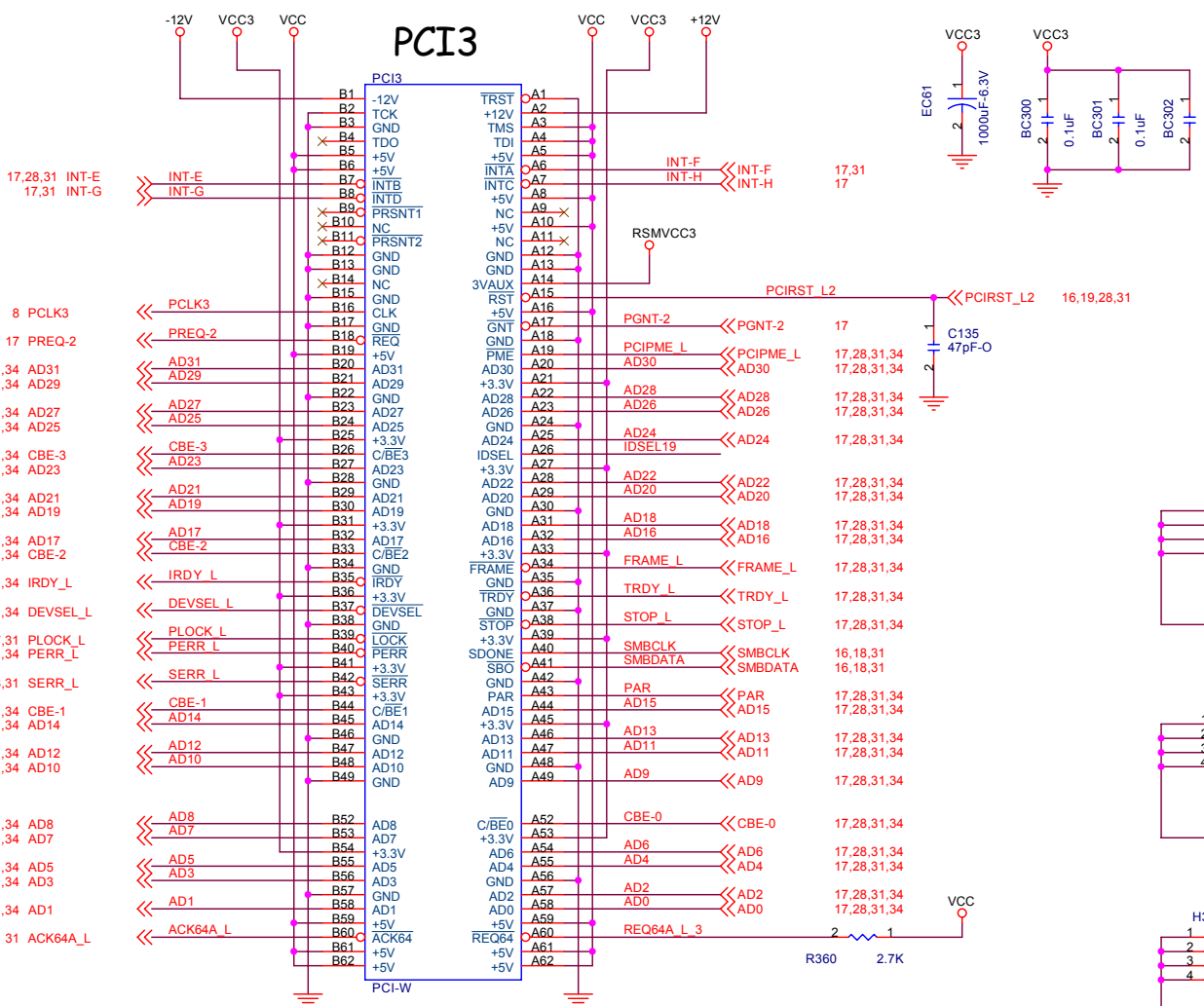
$$VOUT = 0.8V(1 + R_t / R_b)$$

### 3.3V DUAL

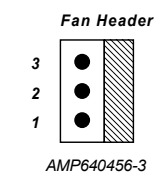
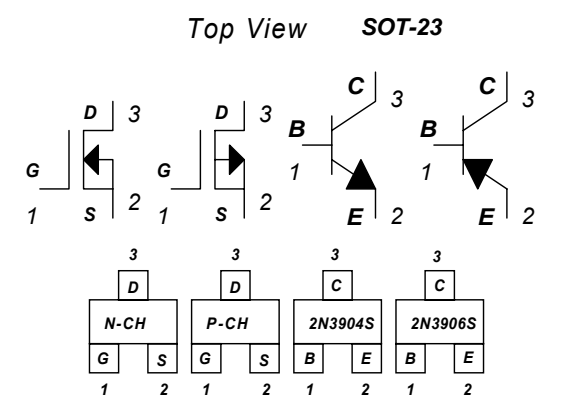
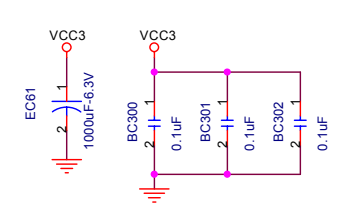
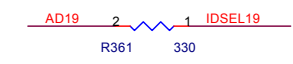
### 2.6V DUAL

VCC26SB needs supply 570mA of current.

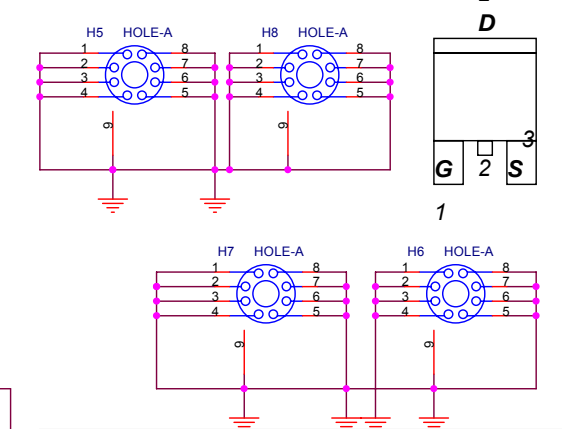
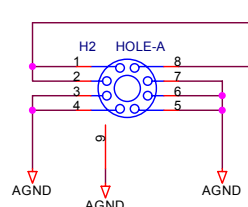
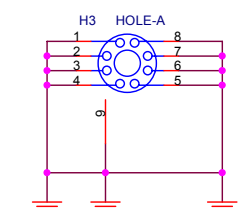
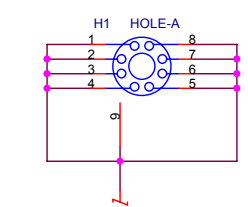
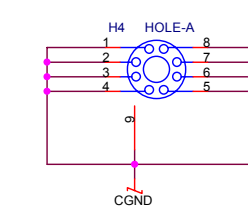
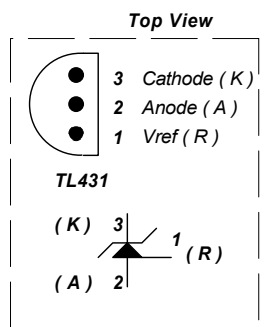
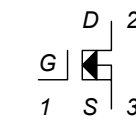




PCI3-INT: IDSEL=AD19  
INTA: INTF REQ=PREQ2#  
INTB: INTF GNT=PGNT2#  
INTC: INTG  
INTD: INTH



TO-263 / TO-252



Title

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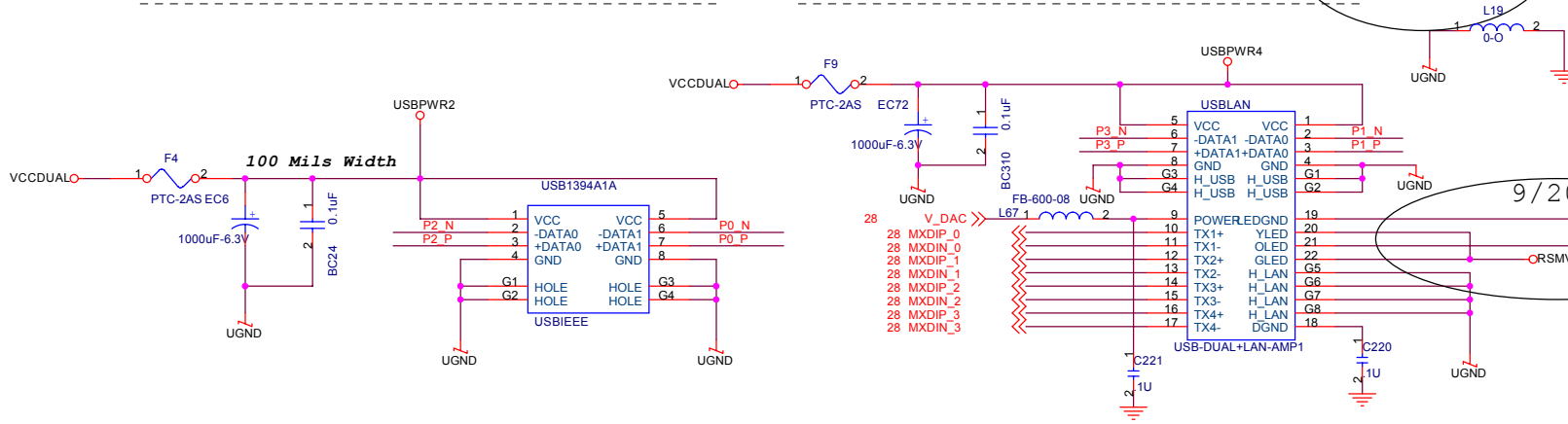
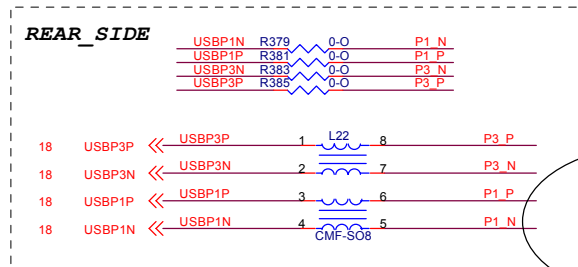
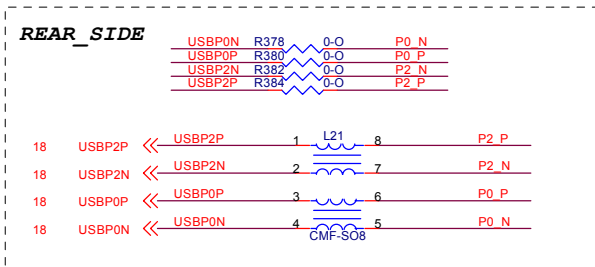
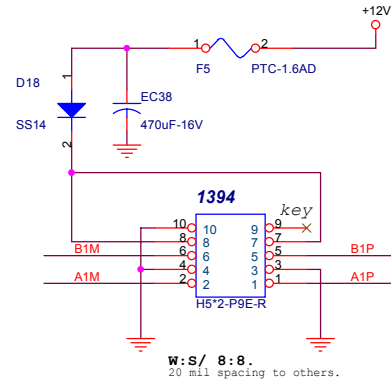
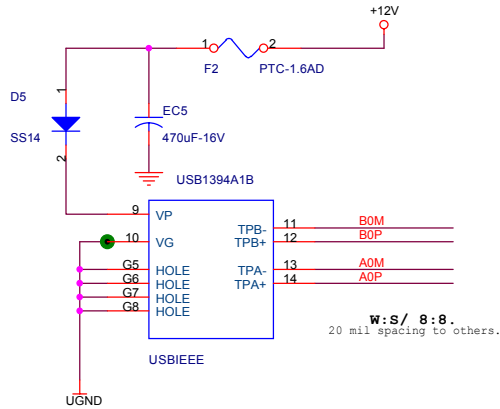
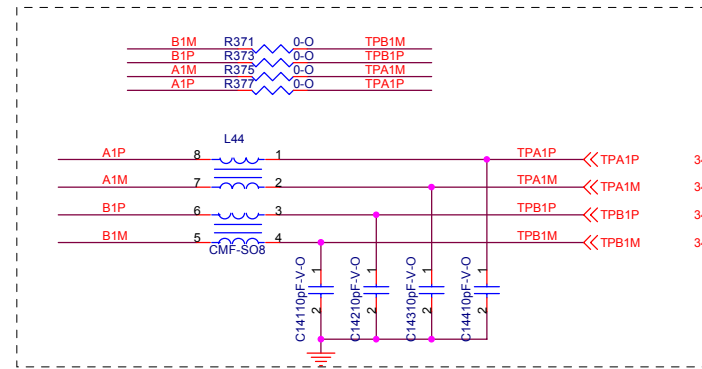
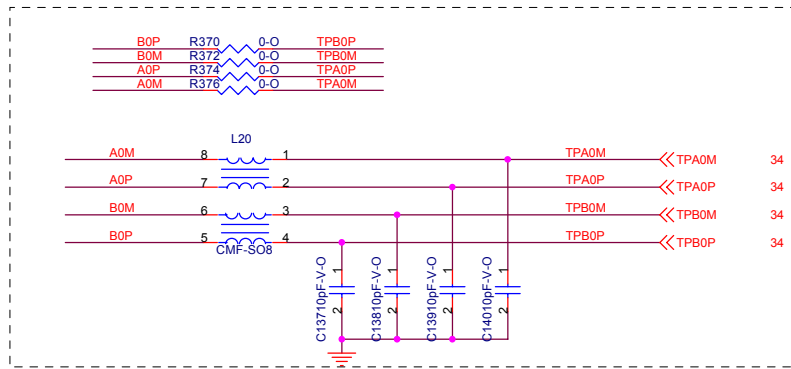
PCI Slot 3

915GV-M5

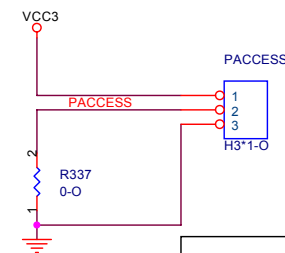
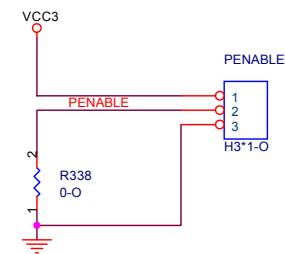
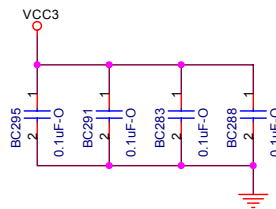
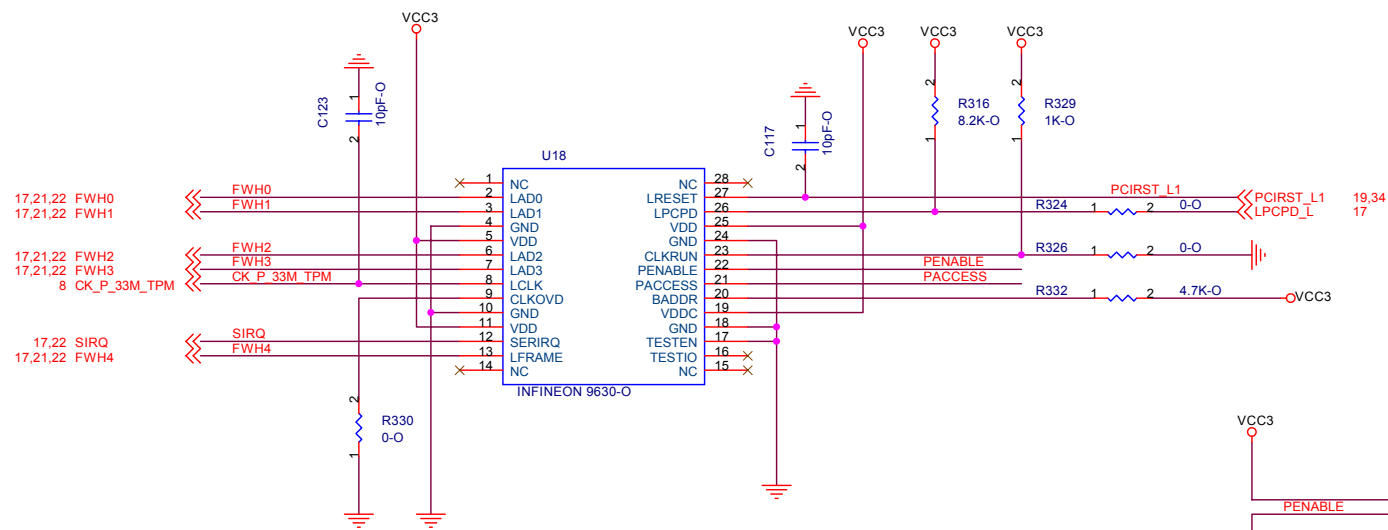
Rev 1.0

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Revision A to Revision B

- 1. R105 & R106 change from Open to 0 ohm 0603, C85 change from Open to 0.01uF 0603, ER89 change from Open to 47 ohm 0603 for system can not boot issue.
- 2. RN21 change from 0 ohm 8P4R to Open, RN22 change from Open to 0 ohm 8P4R for system can not boot issue.
- 3. Add R362 1K ohm 0603 for 2.5V power control issue.
- 4. Add SMI1 header for Legend specifications.
- 5. Add F\_USB1 and F\_USB2 header for Legend specifications.
- 6. Add I2C header for Legend specifications.
- 7. Add SIRQ1 header for Legend specifications.
- 8. Add JPT2 and JPT3 header for Legend specifications.
- 9. Add IRDA header for Legend specifications.
- 10. Change SYSFAN header for Legend specifications.
- 11. Add CDIN2 header for Legend specifications.
- 12. Add F\_AUDIO header for Legend specifications.
- 13. Add F\_PANEL and PSW1 header for Legend specifications.
- 14. Add JP3 and JP4 header for Legend specifications.
- 15. Remove PCIe1 and CNR slots and replace with PCI3 for Legend specifications.
- 16. Add F\_1394 header and V-port capacitors C137~C144 for Legend specifications.
- 17. R10, R17, Q1 change to Open, ER16 change to 1.3K-1% ohm 0603 for giga lan fail issue.
- 18. R86 change to 270K ohm 0603, C57 change to 1000pF 0603 & C40 change to 5600pF 0603 for VCCP PWM gate jittering issue.
- 19. EC2 & EC3 change to 6mm for PCI card installation mechanical issue.

Revision B to Revision 1.0

- 1. EC25 & EC26 change from 470uF 25V to 1000uF 6.3V, EC35 & EC40 change from 1000uF 6.3V to 1800uF 6.3V for 3DMark 2003 hang issue.
- 2. EC46 & EC47 change from 1000uF 6.3V to 1800uF 6.3V for S3/S4 can not burn in issue.
- 3. Add ER126 24K ohm 0603, delete R194, R197, BC134, R188, ER79, C84, ER78, C82, C83, Change ER77 from 7.5K to Open, D17 from 1N4148 to Open, R190 from 10 ohm 0805 to open, D19 from Open to 1N4148 and R191 from Open to 10 ohm 0805 for RT9214 support.
- 4. Change common mode choke RN9, RN10, RN11 AND RN19 to single R370 ~ R385 for SMT issue.